

MODEL NAME : Aventador
PCB NO : LA-D781P
BOM P/N : TBD

	R1	R3	R3	R3
CPN	DAA000CE010	DAA000CE011	DAA000CE012	DAA000CE013



Dell/Compal Confidential

Schematic Document

Aventador (Kabylake Y)

AR Option

UT1 AR_SLL42B	UT1 AR_QST72B	UT1 AR_QT5T0B	UT1 AR_SLLSPB
SA0000996L D8L6340 SLL42 B1	SA0000996L JHLE6340 QST72 C0	SA0000996L JHLE6340 QT5T C1	SA0000996L JHLE6340 SLLSP C1

nVpro CPU Option

UC1 QLD0B	UC1 QLD0B	UC1 QLD0B	UC1 SR2ZX
SA0000452L HEB067702739525 QLDQ	SA0000452L HEB067702739823 QLDH	SA0000452L HEB067702739824 QLD5	SA0000452L HEB067702739823 SR2ZX

Vpro CPU Option

UC1 QLD0B	UC1 QLY7B	UC1 QLY7B
SA0000452L HEB067702739825 QLDV	SA0000452L HEB067702739527 QLY8	SA0000452L HEB067702739526 QLY7

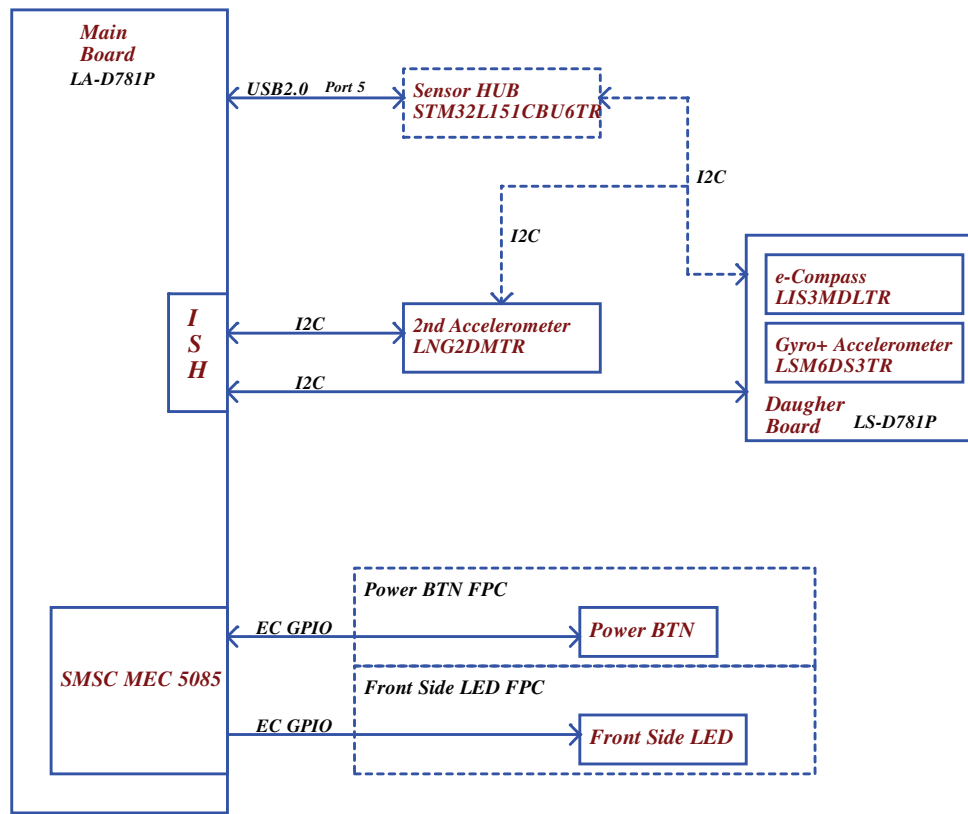
2016-08-31
Rev: A00

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POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF		LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	Power plane	+3VALW_DS _W +5VALW +3VALW +3VLP	+3V_PCH +1.8V_PRIM +1.0V_PRIM +1.0VA_GATE +VCC_PRIM	+1.2V_DDR +3.3V_CV2 +1.8V_MEM +1.0V_VCCST	+5VS +1.8VS +1.0V_VCCSTG +0.85VS_VCCIO +0.6VS_VTT +VCC_SA +VCC_GT +VCC_CORE
S0		ON	ON	ON	ON
S3 / AC		ON	ON	ON	OFF
DS3		ON	OFF	ON	OFF
S5 S4/AC		ON	OFF	OFF	OFF
S5 S4/AC doesn't exist		OFF	OFF	OFF	OFF

Control Table

		MEC5085	BATT	XD	USH	TI PD	CCG4	ECE1117	AMP	Charger
SMLOCLK SMLODATA	PCH									
SMIL1_SMBCLK SMIL1_SMBDATA	PCH	V								
SMBCLK SMBDATA	PCH			V						
MCP23017_SMBDAT MCP23017_SMBCLK	MEC5085							V		
UPD_SMBDAT UPD_SMBCLK	MEC5085					V				
EC_I2C_CLK EC_I2C_DAT	MEC5085								V	
PBAT_SMBCLK PBAT_SMBDAT	MEC5085		V							
CCG4_I2C_CLK CCG4_I2C_DATA	MEC5085						V			
CHARGER_SMBCLK CHARGER_SMBDAT	MEC5085									V

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	PCB Revision	REV
0	240K +/- 5%	4700p	0.1	EVT1.0
1	130K +/- 5%	4700p	0.2	DVT1.0/DVT1.1
2	62K +/- 5%	4700p		
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

SOC DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

SOC PCIe Port Mapping	PCI EXPRESS	DESTINATION
	Lane 1	Alpine Ridge
	Lane 2	
	Lane 3	
	Lane 4	
	Lane 5	NGFF (SSD)
	Lane 6	
	Lane 7	
	Lane 8/ SATA 1	
	Lane 9	Cardreader
Lane 10	WLAN	

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	Alpine Ridge
	CLKOUT_PCIE2	WLAN
	CLKOUT_PCIE3	SDD
	CLKOUT_PCIE4	Card Reader
CLKOUT_PCIE5		

USB 3.0 PORT#	DESTINATION
1	USB DP MUX
2	USB Debug
3	
4	

USB 2.0 PORT#	DESTINATION
1	USB Type C (nAR)
5	Sensor Hub
7	Fingerprint
3	Touch Panel
9	CAM & IR CAM
2	NGFF(WLAN)

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	LPC Debug

Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

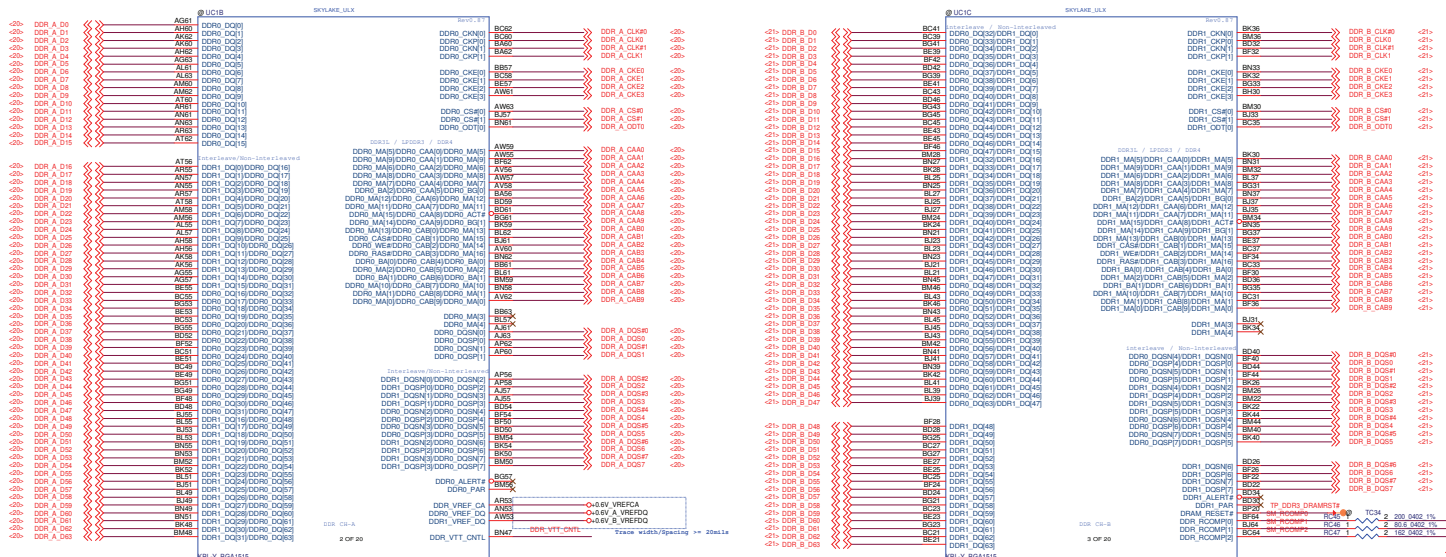
⏏ : means Analog Ground

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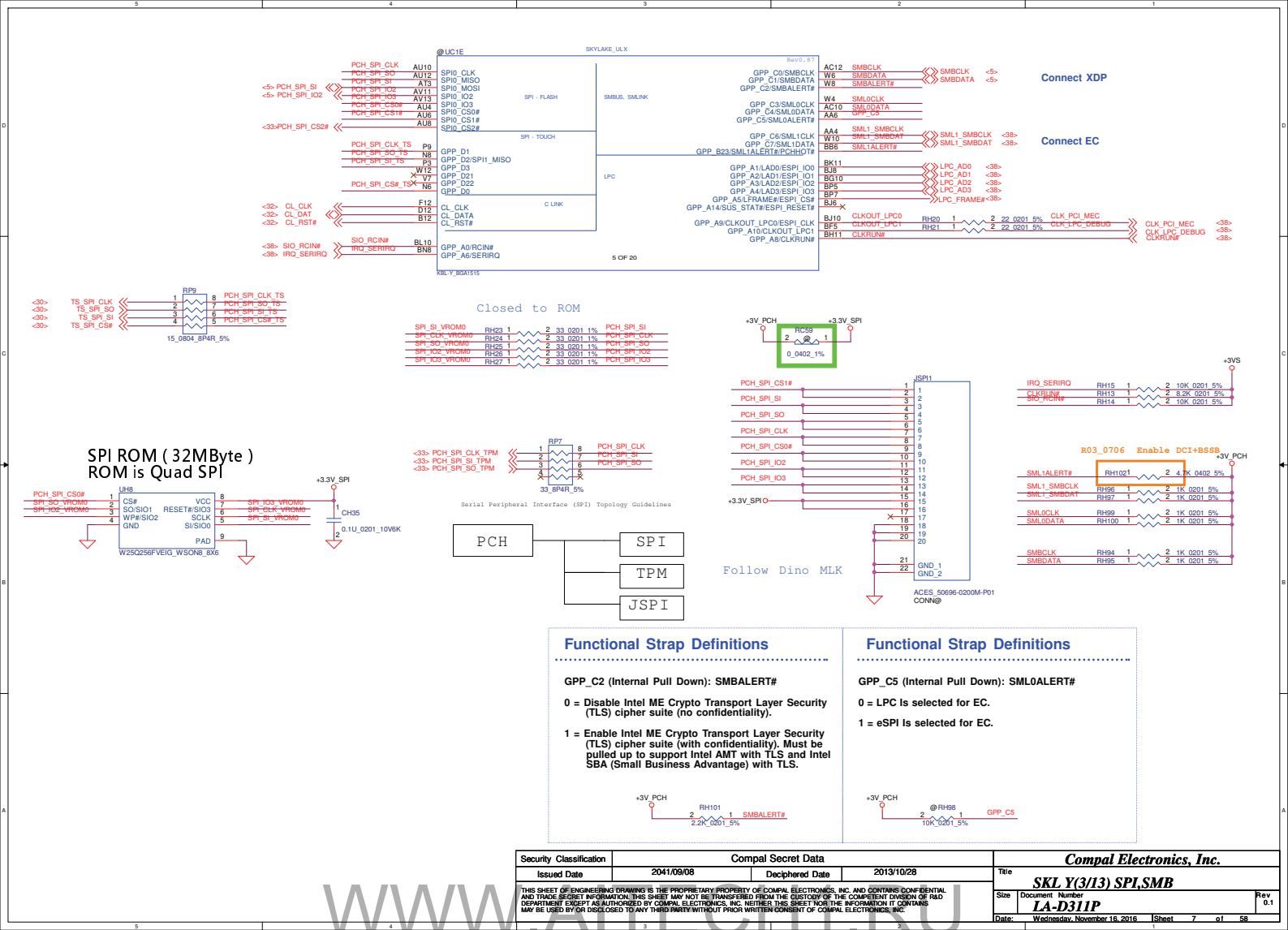
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Non-Interleave Memory



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2041/09/06		2013/10/26		2041/09/06	

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Functional Strap Definitions

GPP_B14 (Internal Pull Down): SPKR

TOP Swap Override

0 = Disable TOP Swap mode, AAU30 Use

1 = Enable TOP Swap Mode.



UC11 SKYLAKE_ULX

Rev0.01

CS12_DN0

CS12_DN1

CS12_DN2

CS12_DN3

CS12_DN4

CS12_DN5

CS12_DN6

CS12_DN7

CS12_DN8

CS12_DN9

CS12_DN10

CS12_DN11

CS12_DN12

CS12_DN13

CS12_DN14

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CS12_DN75

CS12_DN76

CS12_DN77

CS12_DN78

CS12_DN79

CS12_DN80

CS12_DN81

CS12_DN82

DDR Memory Configuratio Type Strap pin

Rev0.01

MEM_CONFIG0

MEM_CONFIG1

MEM_CONFIG2

MEM_CONFIG3

MEM_CONFIG4

MEM_CONFIG5

MEM_CONFIG6

MEM_CONFIG7

MEM_CONFIG8

MEM_CONFIG9

MEM_CONFIG10

MEM_CONFIG11

MEM_CONFIG12

MEM_CONFIG13

MEM_CONFIG14

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MEM_CONFIG70

MEM_CONFIG71

MEM_CONFIG72

MEM_CONFIG73

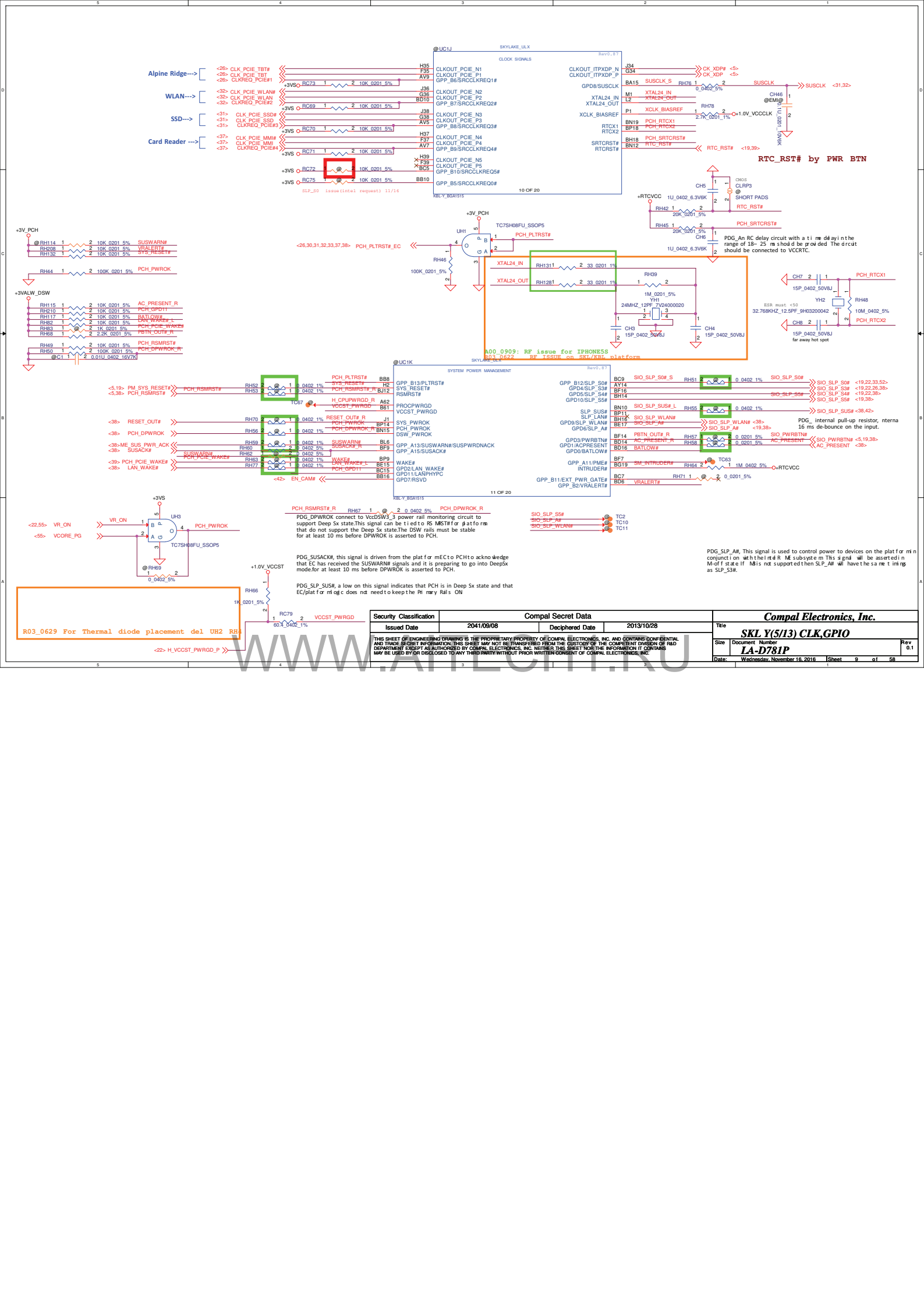
MEM_CONFIG74

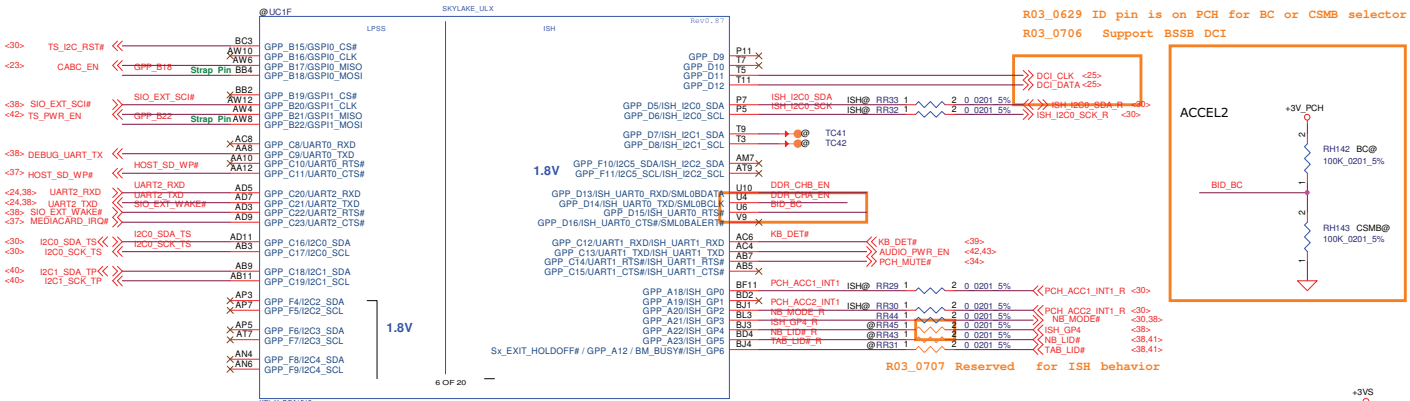
MEM_CONFIG75

MEM_CONFIG76

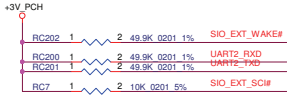
Pin Name	Micron 4GB SA4000BFF3L	Micron 8GB SA4000BFF3L	Micron 16GB SA4000BFF3L	Rynix 4GB SA4000BFF3L	Rynix 8GB SA4000BFF3L	Rynix 16GB SA4000BFF3L	Samsung 4GB SA4000BFF3L	Samsung 8GB SA4000BFF3L	Samsung 16GB SA4000BFF3L
MEM_CONFIG0	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0
MEM_CONFIG2	0	0	0	0	1	1	1	1	0
MEM_CONFIG3	0	0	0	0	0	0	0	0	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0

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R03_0622 Del RC286,RC287 change power rail to +3V_TS



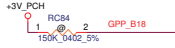
Functional Strap Definitions

GPP_B18 (Internal Pull Down): GSSPIO_MOSI

No Reboot

0 = Disable No Reboot mode -> AAU30 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/IDP.



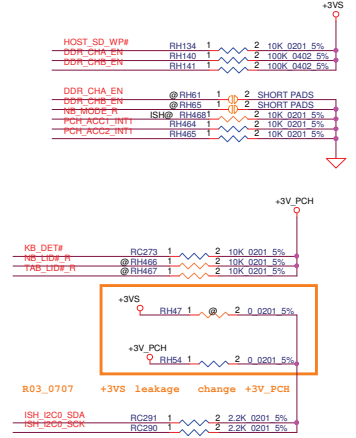
Functional Strap Definitions

GPP_B22 (Internal Pull Down): GSSPI1_MOSI

Boot BIOS Strap Bit

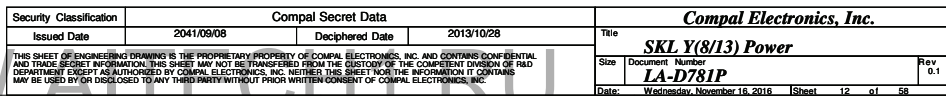
0 = SPI Mode -> AAU30 Use

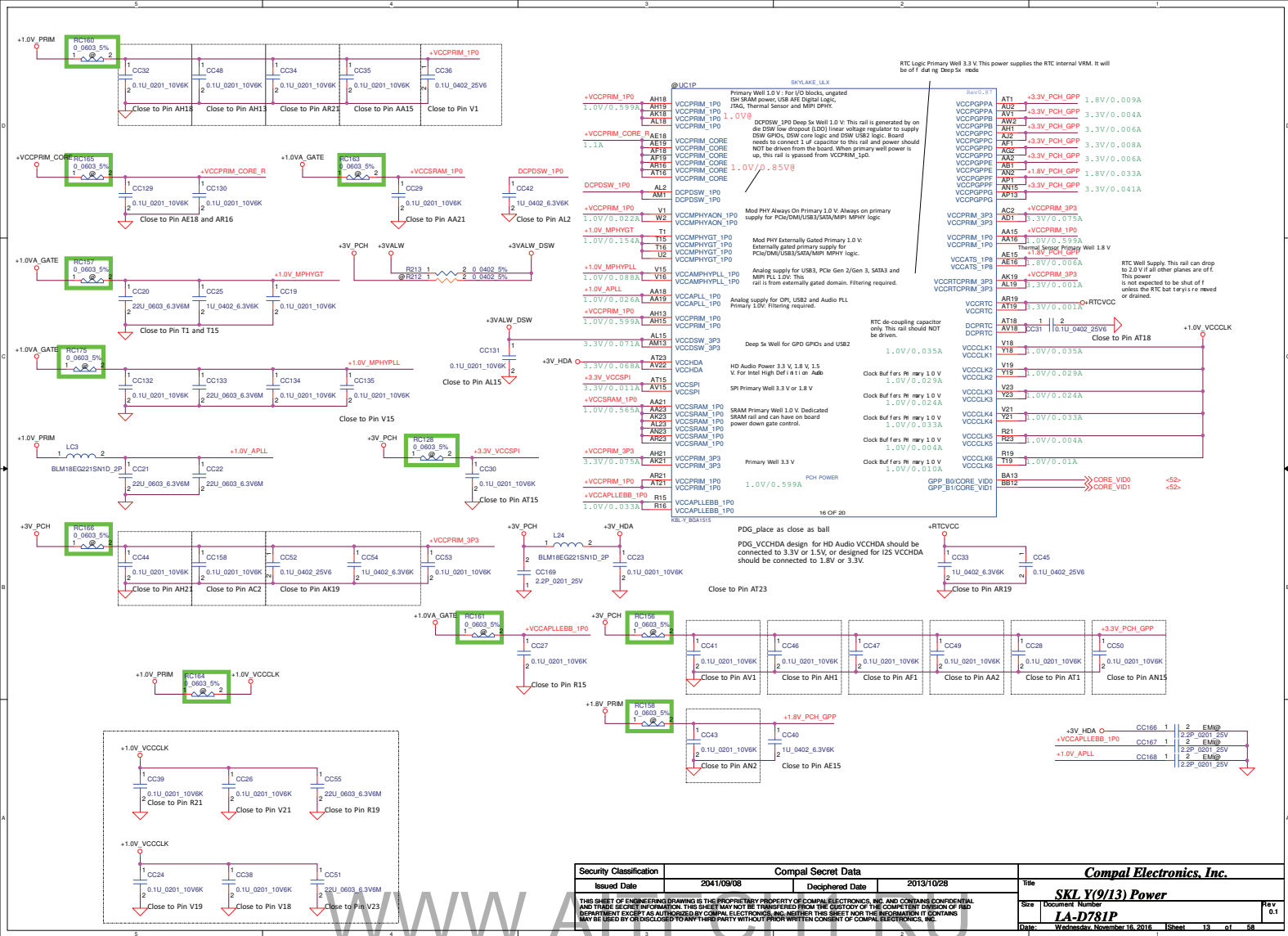
1 = LPC Mode

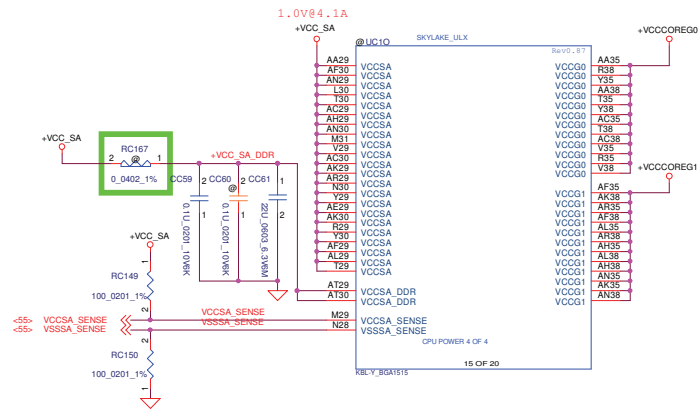


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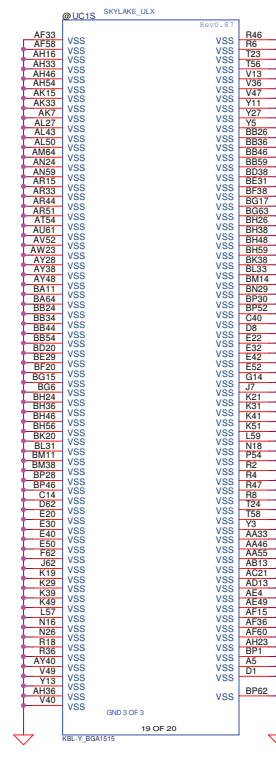








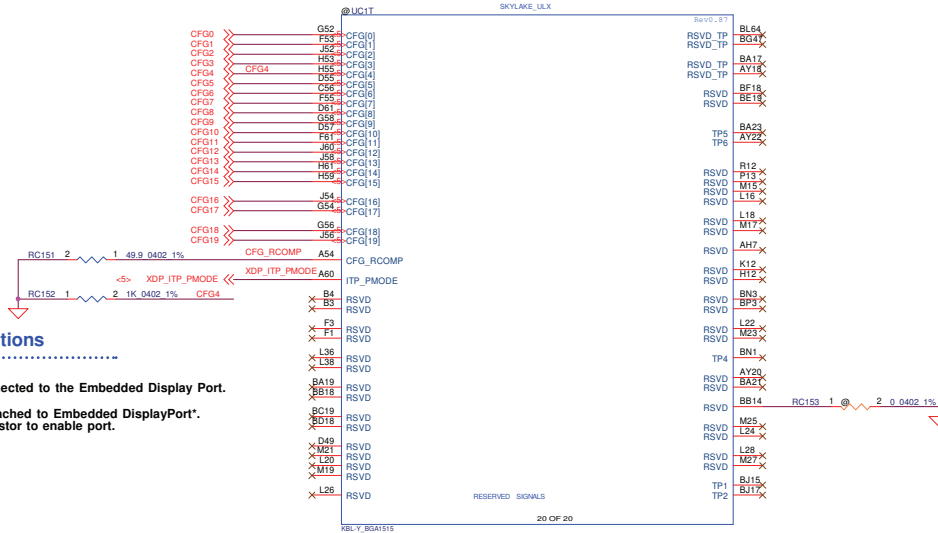
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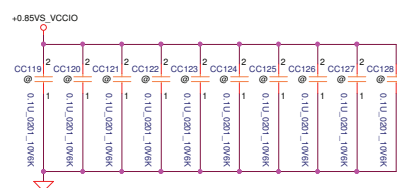
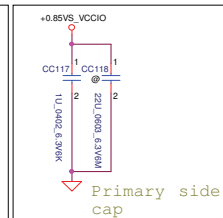
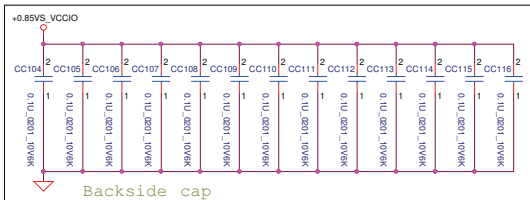
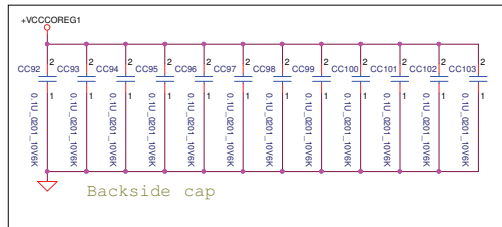
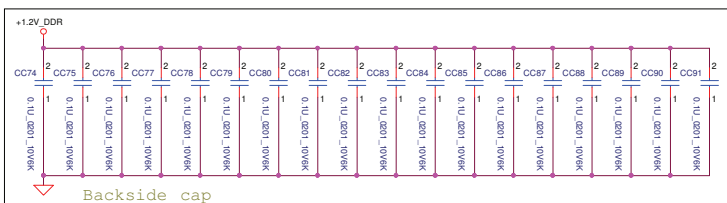
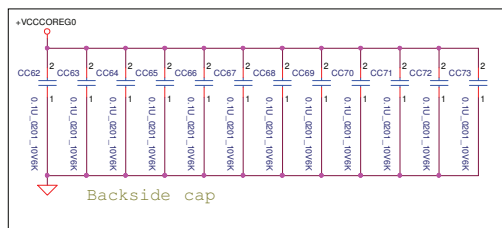
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Functional Strap Definitions

CFG[4] : Display Port Presence strap
0 = Enabled - A Display Port device is connected to the Embedded Display Port.
No connect for disable.
1 = Disabled - No Physical Display Port attached to Embedded DisplayPort*.
Pull-down to GND through a 1 K \pm 5% resistor to enable port.



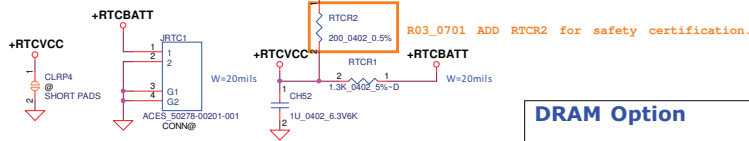
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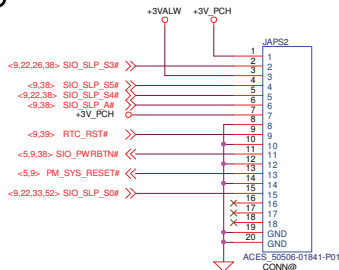
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RTC



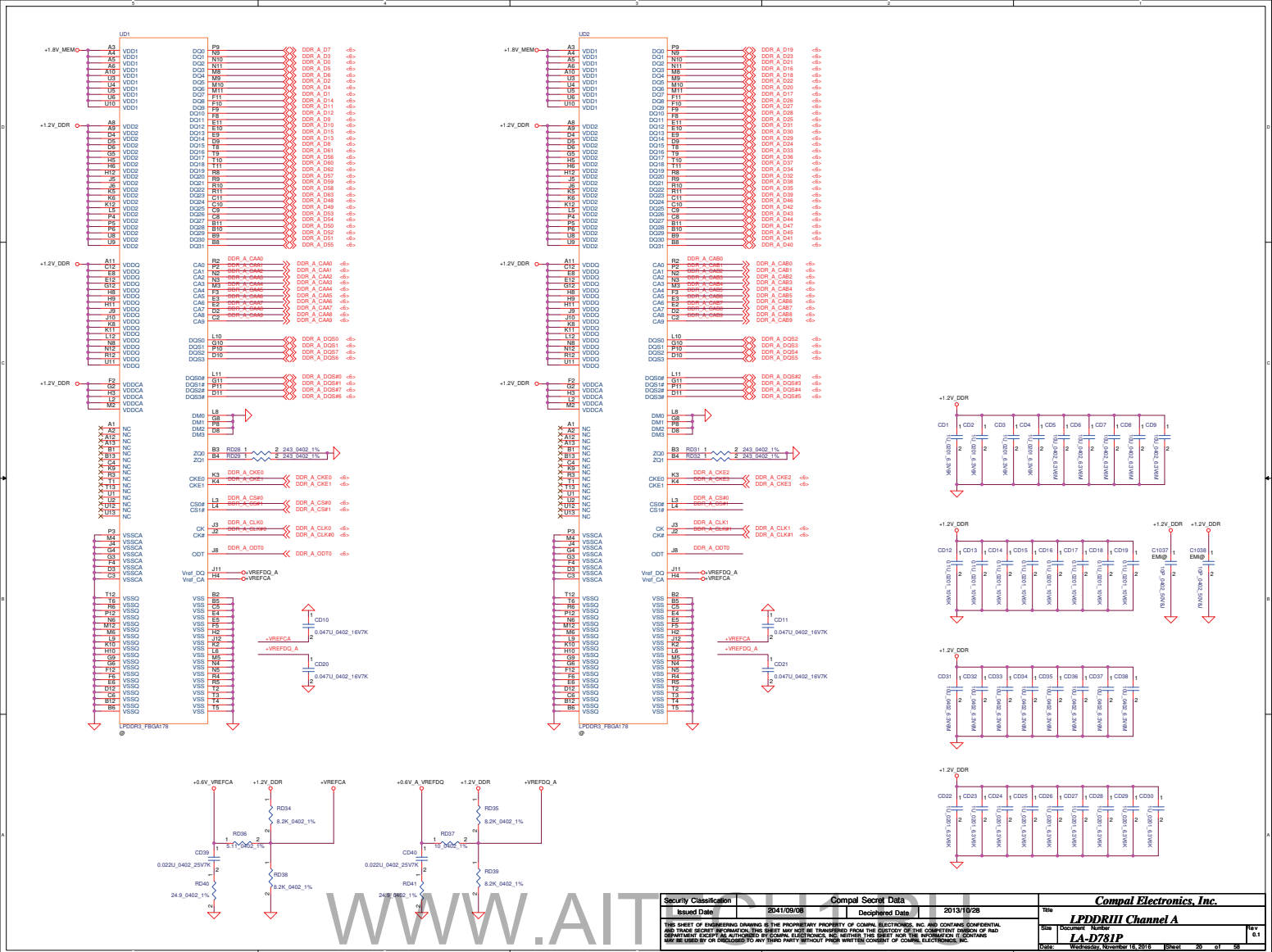
APS

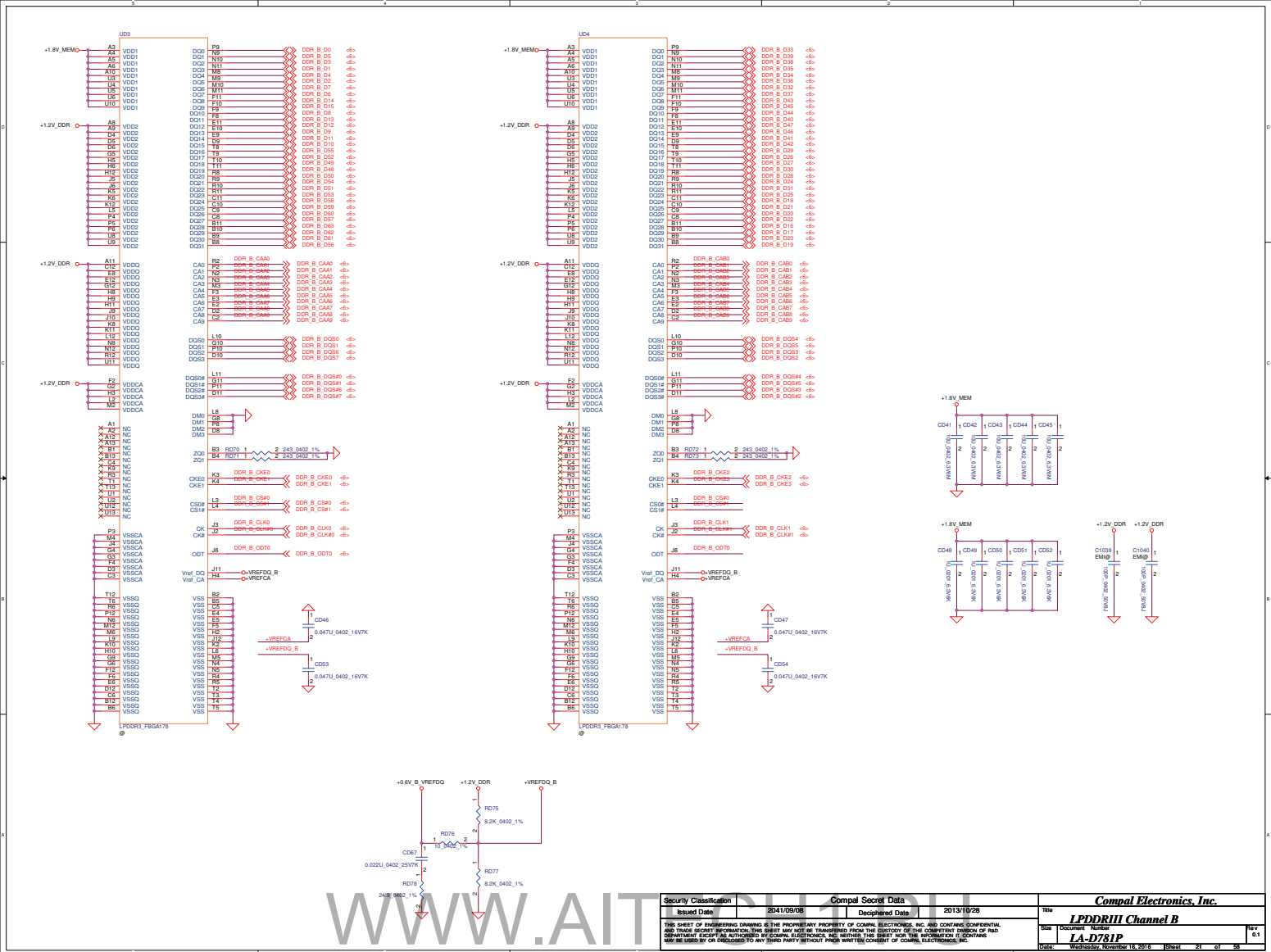


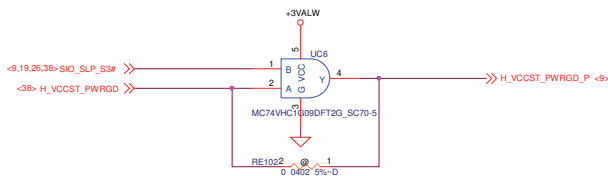
DRAM Option		DRAM Config Option				X76
		MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	
Micron 4G/1866		X76_M4G@ UD1 MT52L125M32D1PF-107W SA00009XUJL	X76_M4G@ UD2 MT52L125M32D1PF-107W SA00009XUJL	X76_M4G@ UD3 MT52L125M32D1PF-107W SA00009XUJL	X76_M4G@ UD4 MT52L125M32D1PF-107W SA00009XUJL	X7666031L03
Micron 8G/1866		X76_M8G@ UD1 MT52L125M32D2PF-107W SA00009XUJL	X76_M8G@ UD2 MT52L125M32D2PF-107W SA00009XUJL	X76_M8G@ UD3 MT52L125M32D2PF-107W SA00009XUJL	X76_M8G@ UD4 MT52L125M32D2PF-107W SA00009XUJL	X7666031L06
Micron 16G/1866		X76_M16G@ UD1 MT52L1G32D4PG-107WT SA00009XUJL	X76_M16G@ UD2 MT52L1G32D4PG-107WT SA00009XUJL	X76_M16G@ UD3 MT52L1G32D4PG-107WT SA00009XUJL	X76_M16G@ UD4 MT52L1G32D4PG-107WT SA00009XUJL	X7666031L09
Hynix 4G/1866		X76_H4G@ UD1 H5CCNNNBUTMLAR-NUD SA00008G60L	X76_H4G@ UD2 H5CCNNNBUTMLAR-NUD SA00008G60L	X76_H4G@ UD3 H5CCNNNBUTMLAR-NUD SA00008G60L	X76_H4G@ UD4 H5CCNNNBUTMLAR-NUD SA00008G60L	X7666031L01
Hynix 8G/1866		X76_H8G@ UD1 H5CCNNNBUTMLAR-NUD SA00008FJ0L	X76_H8G@ UD2 H5CCNNNBUTMLAR-NUD SA00008FJ0L	X76_H8G@ UD3 H5CCNNNBUTMLAR-NUD SA00008FJ0L	X76_H8G@ UD4 H5CCNNNBUTMLAR-NUD SA00008FJ0L	X7666031L04
Hynix 16G/1866		X76_H16G@ UD1 H5CCNNNBUTMLAR-NUD SA00008Y70L	X76_H16G@ UD2 H5CCNNNBUTMLAR-NUD SA00008Y70L	X76_H16G@ UD3 H5CCNNNBUTMLAR-NUD SA00008Y70L	X76_H16G@ UD4 H5CCNNNBUTMLAR-NUD SA00008Y70L	X7666031L07
Samsung 4G/1866		X76_S4G@ UD1 K4E8E324EB-EGCF SA00009XY0L	X76_S4G@ UD2 K4E8E324EB-EGCF SA00009XY0L	X76_S4G@ UD3 K4E8E324EB-EGCF SA00009XY0L	X76_S4G@ UD4 K4E8E324EB-EGCF SA00009XY0L	X7666031L02
Samsung 8G/1866		X76_S8G@ UD1 K4E8E304EB-EGCF SA00008QV2L	X76_S8G@ UD2 K4E8E304EB-EGCF SA00008QV2L	X76_S8G@ UD3 K4E8E304EB-EGCF SA00008QV2L	X76_S8G@ UD4 K4E8E304EB-EGCF SA00008QV2L	X7666031L05
Samsung 16G/1866		X76_S16G@ UD1 K4E8E304EB-EGCF SA00008X11L	X76_S16G@ UD2 K4E8E304EB-EGCF SA00008X11L	X76_S16G@ UD3 K4E8E304EB-EGCF SA00008X11L	X76_S16G@ UD4 K4E8E304EB-EGCF SA00008X11L	X7666031L08

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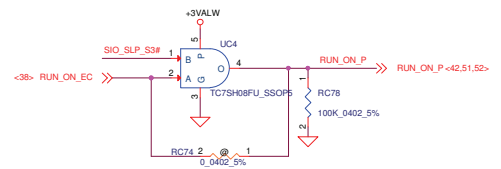
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	RTC, Debug, RAM setting
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				Date	LA-D781P
				Wednesday, November 16, 2016	Sheet 19 of 58



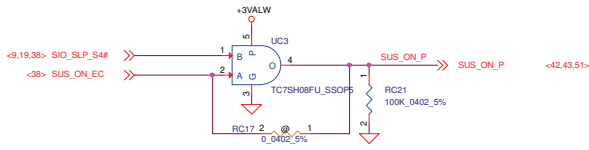




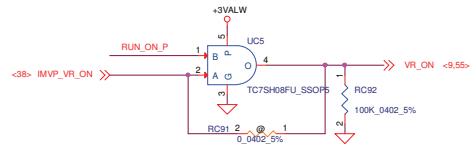
Change CPU VCCST_PWRGD enable from EC & PCH



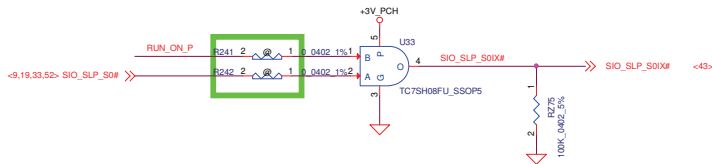
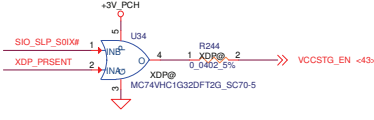
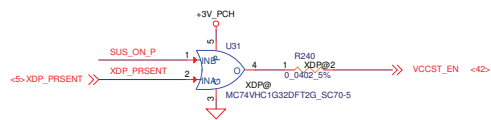
Change VCCIO & VCCSTG power enable from EC & PCH



Change VCCST & 1.2_VR power enable from EC & PCH

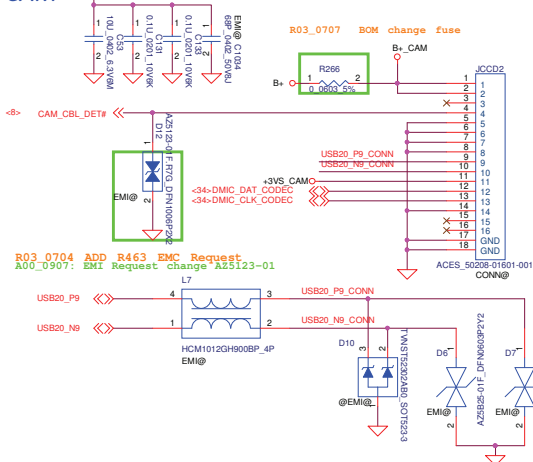


Change VCORE power enable from EC & PCH

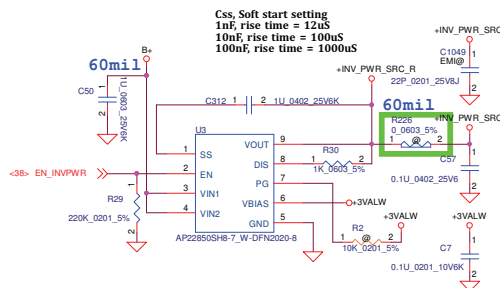


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				Size Document Number
				LA-D781P
Date	Wednesday, November 16, 2016	Sheet	22	of 58

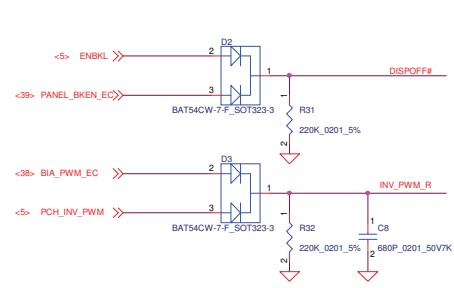
CAM



eDP Backlight Power



BackLight PWM Control



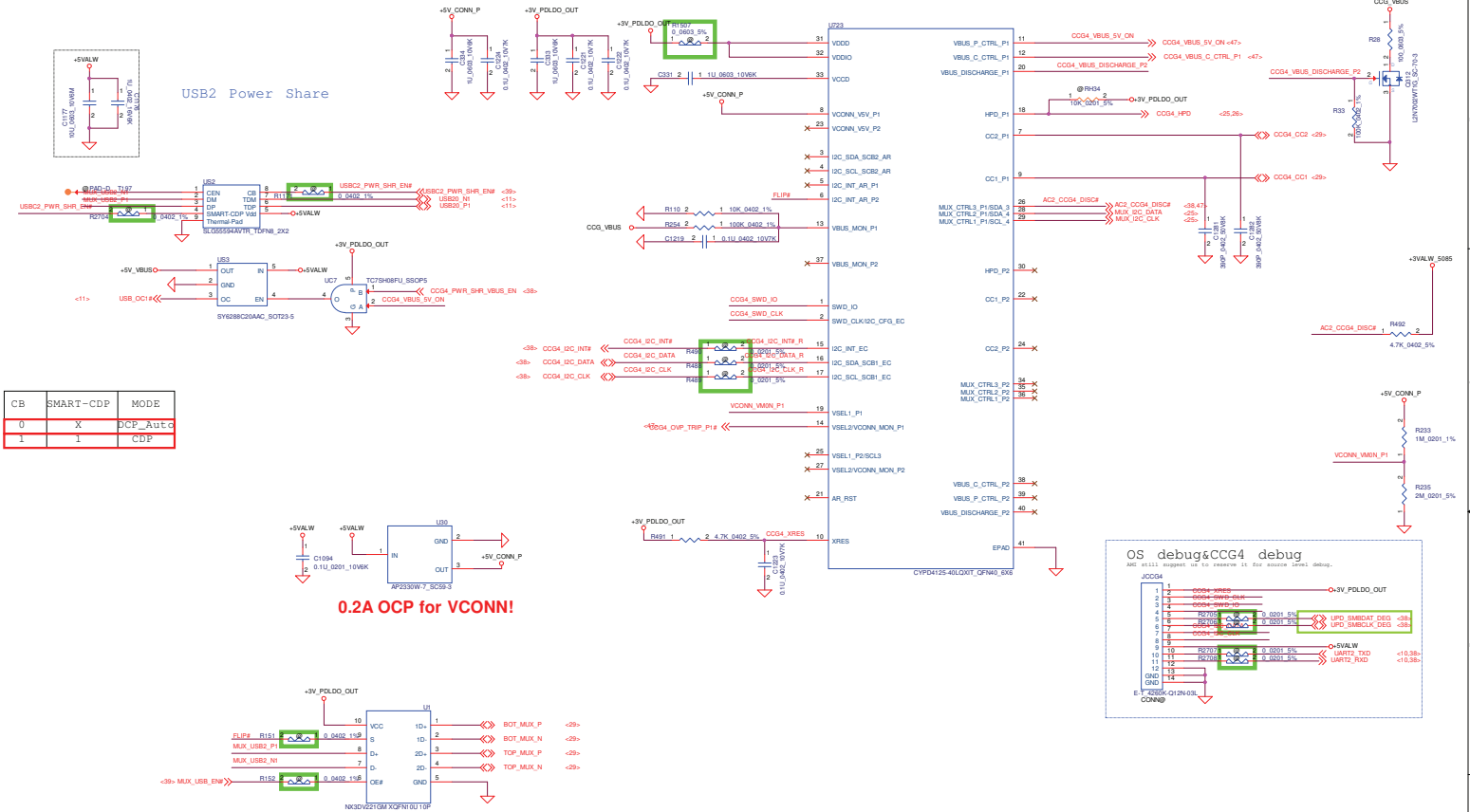
eDP Conn



0.010 0.015K 0.015K eDP_AUX2_C IP23 0.020 5% eDP_AUX2_CONN

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			Sheet	23 of 58
			Rev	0.1

USB2 Power Share



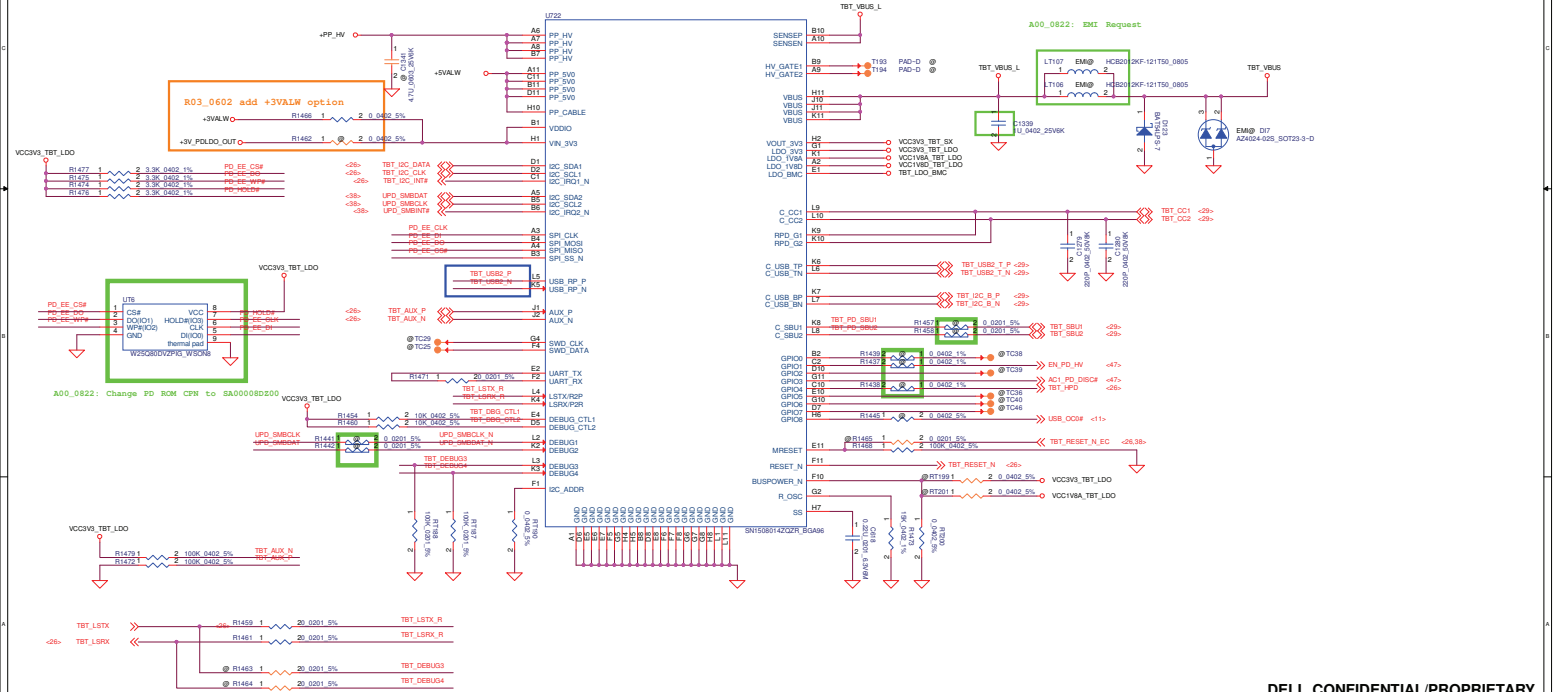
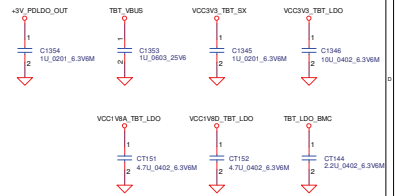
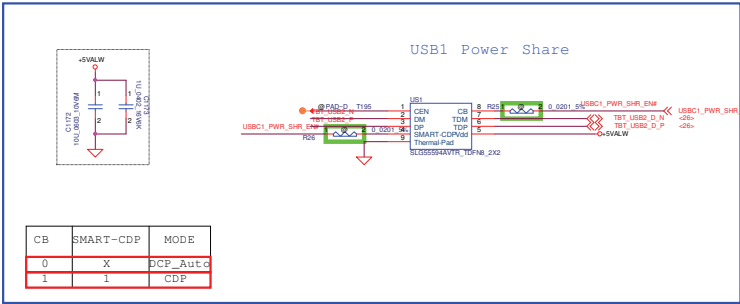
0.2A OCP for VCONN!

FLIP#	MUX_USB_EN#	A_OUT (TOP)	B_OUT (BOT)
X	H	X	X
0	L, D=1D	X	USB
1	L, D=2D	USB	X

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2041/09/08	Declassified Date
Declassified Date	2013/10/26	2013/10/26
Doc No	LA-D781P	Doc No
Rev	01	Rev
Date	Wednesday, November 18, 2015	Date
Page	24	Page
of	58	of

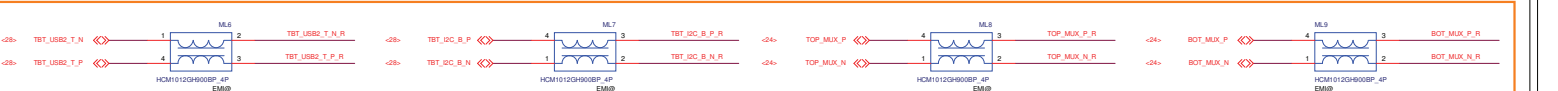
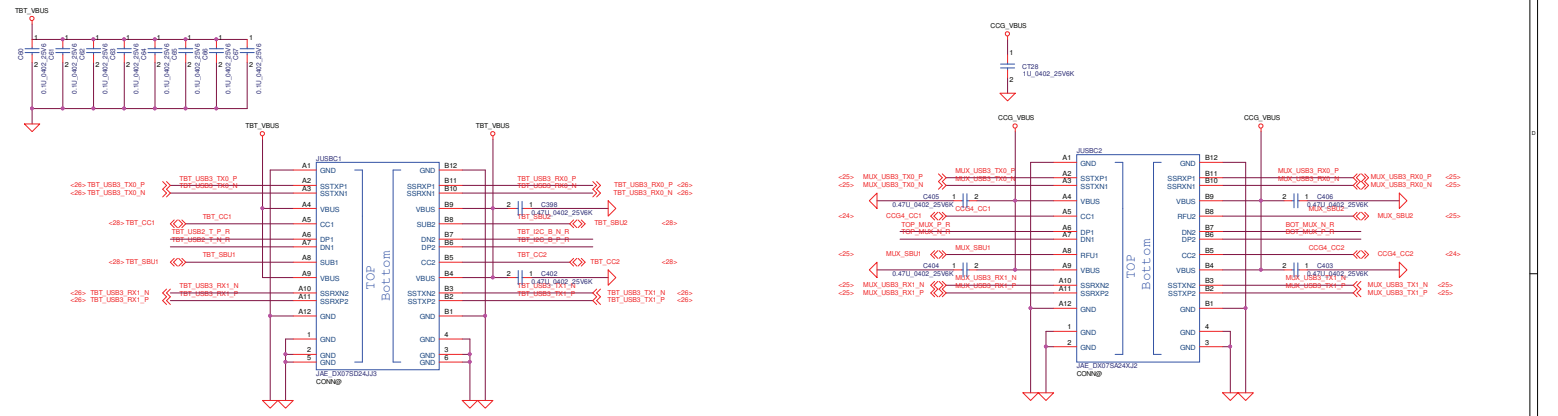


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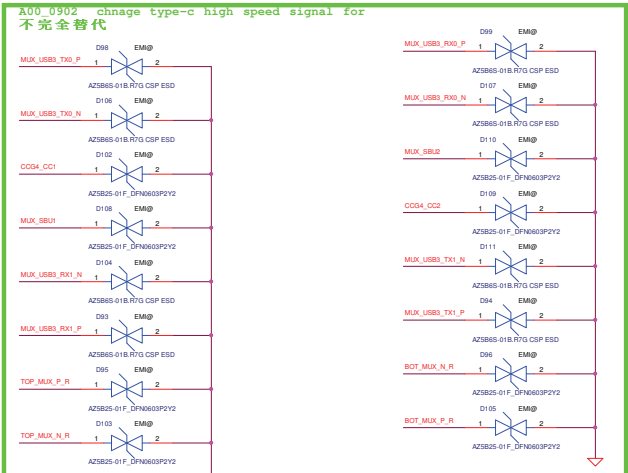
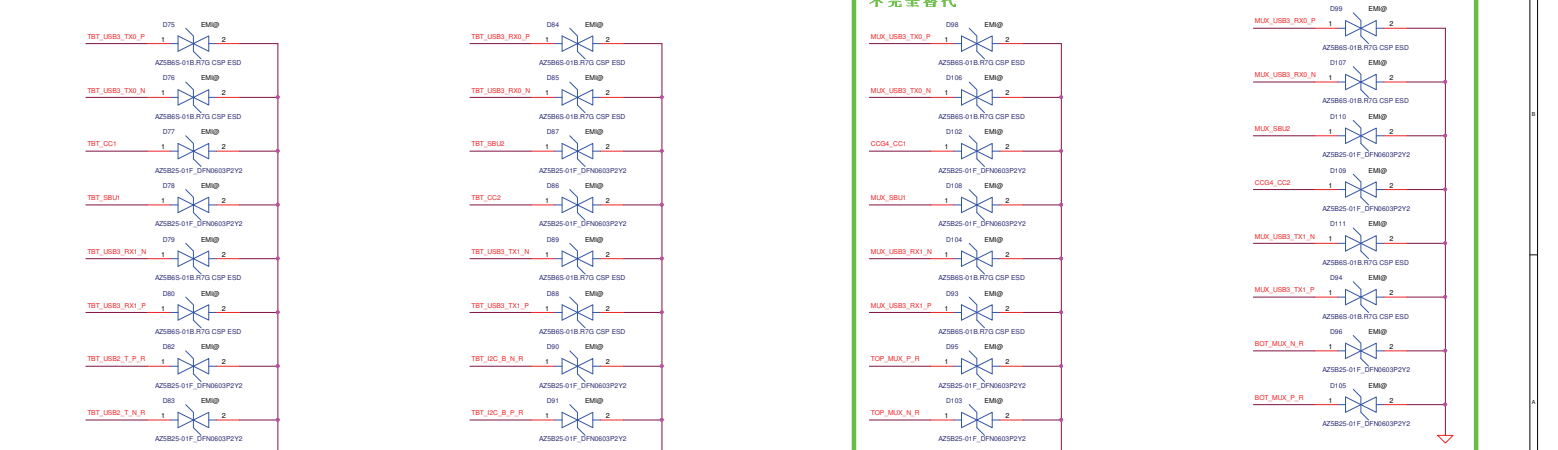


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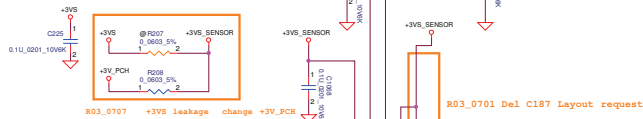
R03_0622 remove co-lay R03_0627 Pin3/Pin2 swap; Pin4/Pin1 swap



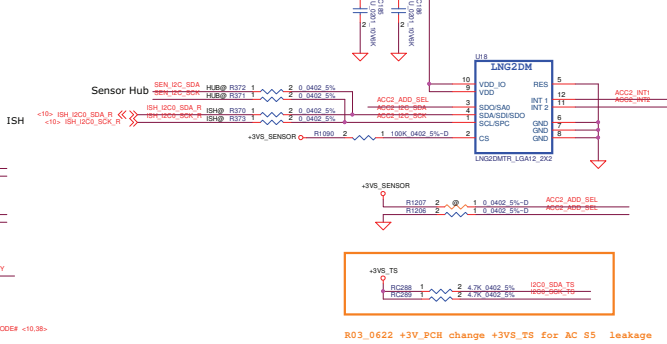
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								P42-PD USB TYPE-C			
Doc No		LA-D781P		Date		Wednesday, November 16, 2016		Page		25 of 36	

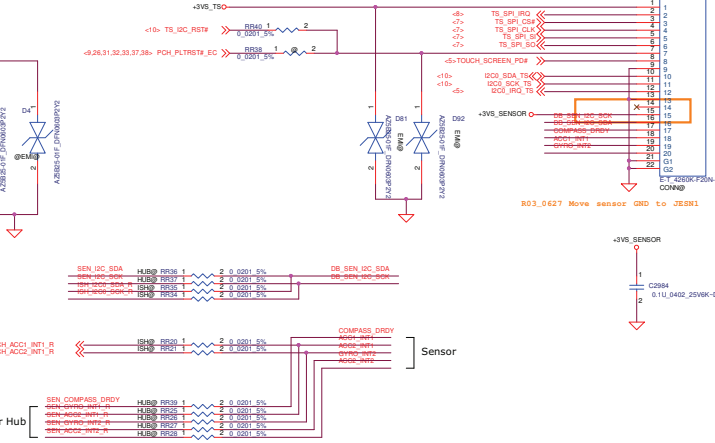
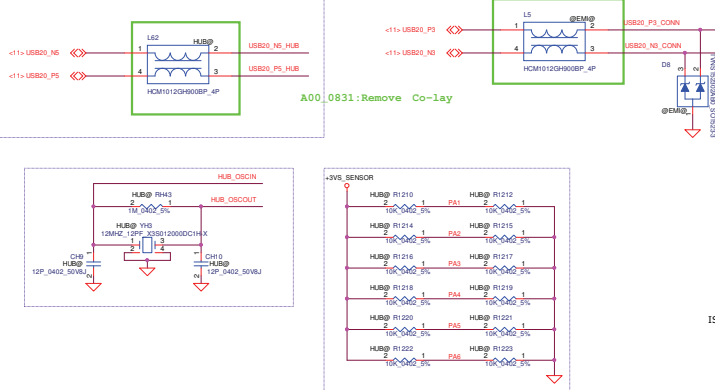
Sensor Hub



2nd Accelerometer



Touch Screen





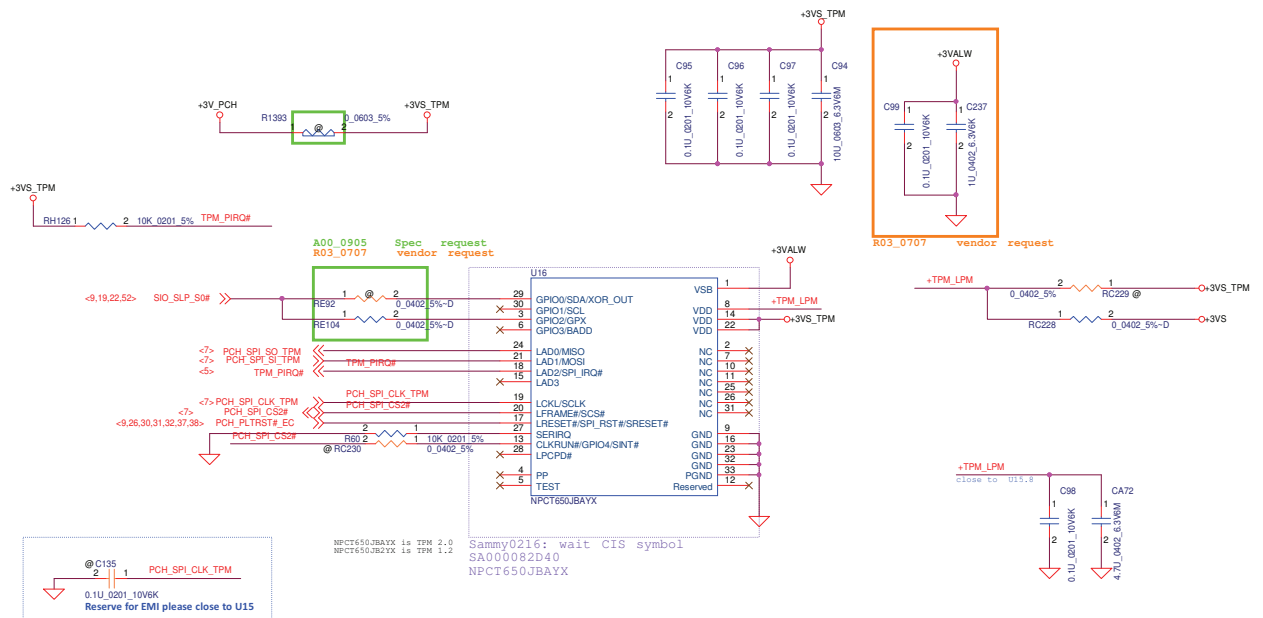
CONFIDENTIAL/PROPRIETARY
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Title		P30-SSD(M.2) / FAN	
Size	Document	Number	
C		LA-D781P	



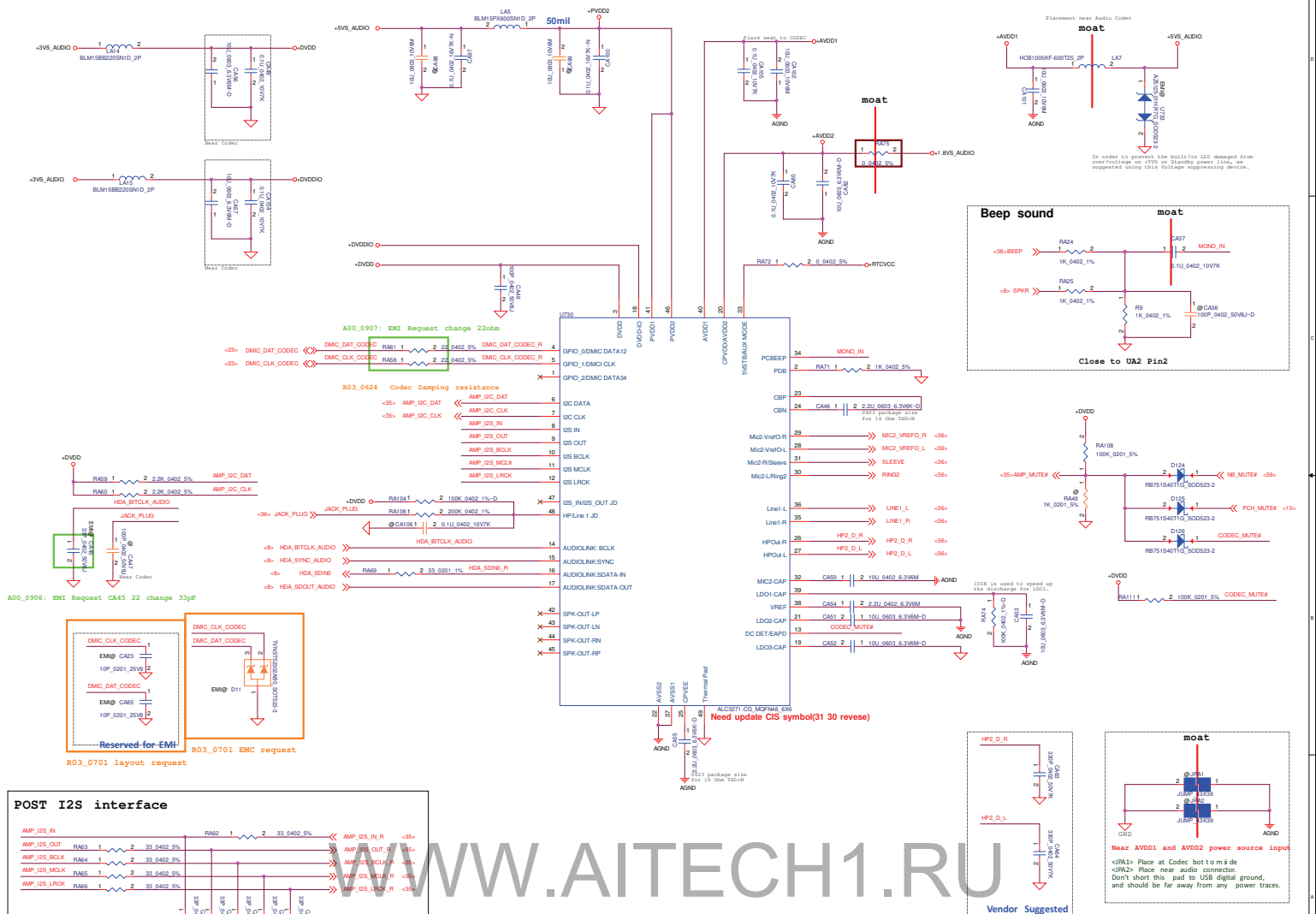
Size	Document Number	Rev
	LA-D781P	0.1
Date:	Wednesday, November 18, 2015	Sheet 32 of 58

NOTE:
Place 0.1 uF capacitors as close as possible to the device power pins

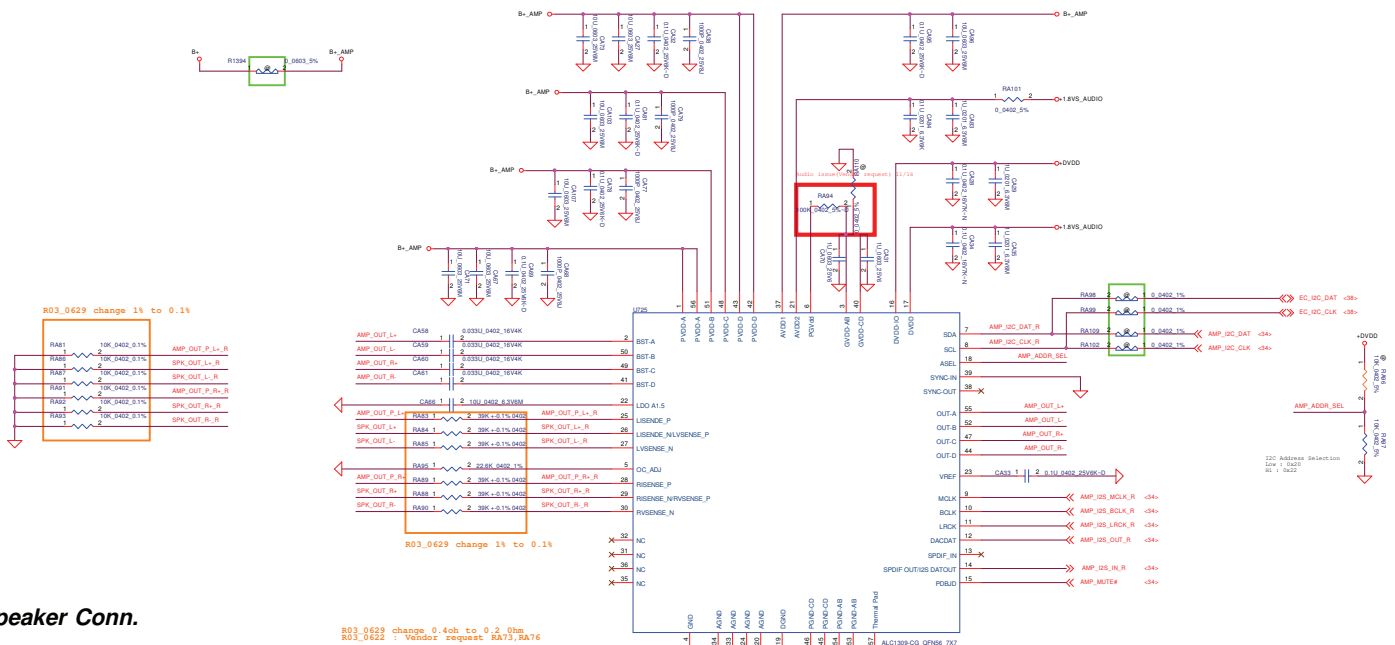


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				Date:	Wednesday, November 16, 2016 Sheet 33 of 58

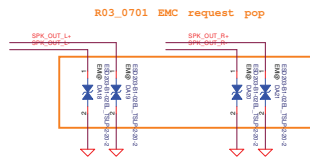
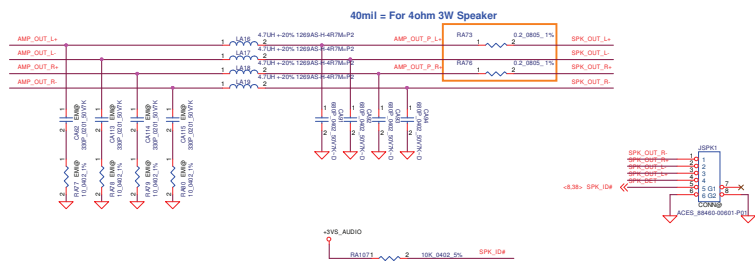
HD Audio Codec



Security Classification	Compul Secret Data		DECLASSIFICATION AUTHORITY: 15X2100	
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SMART AMP

Int. Speaker Conn.



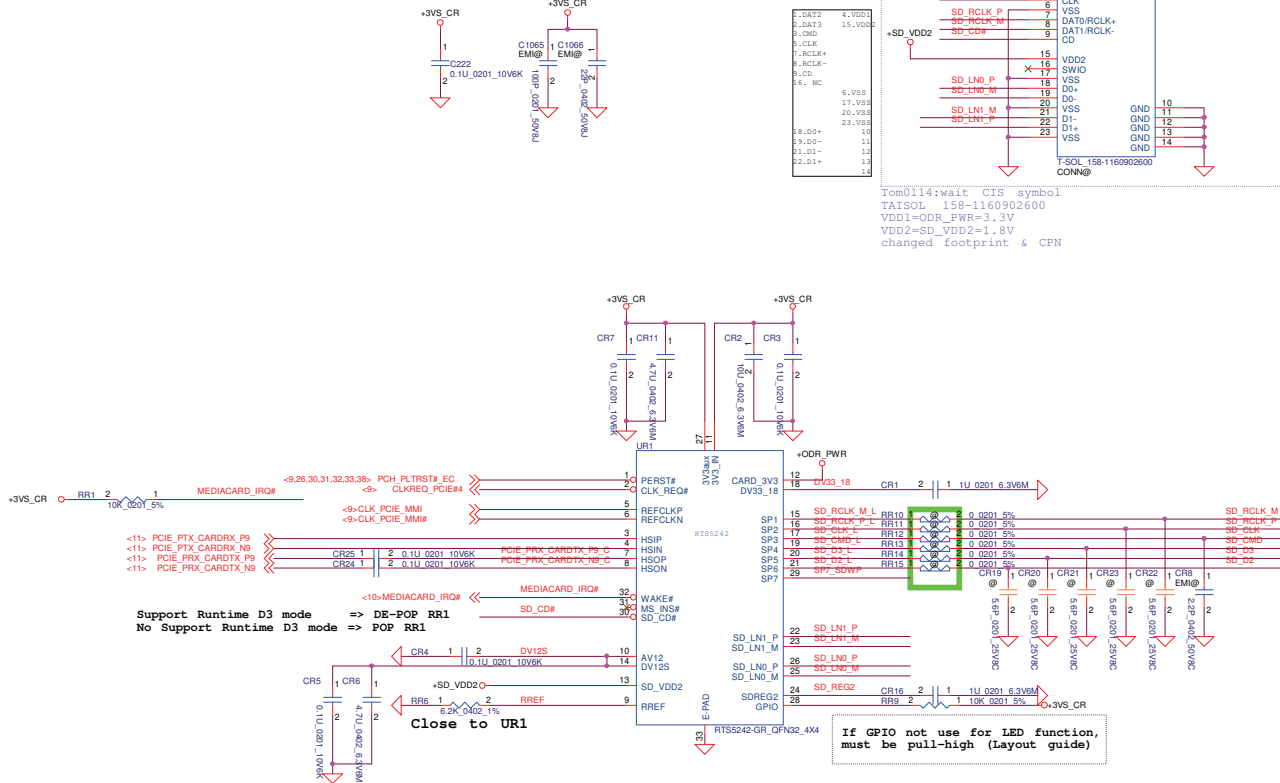
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<p>LA-D781P</p>			<p>Rev 0.1</p>	
<p>Date: 2015/10/28 10:10:28</p>			<p>Sheet 35 of 36</p>	

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	Deciphered Date	

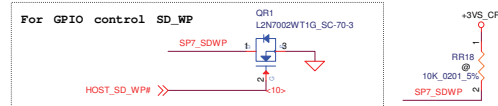
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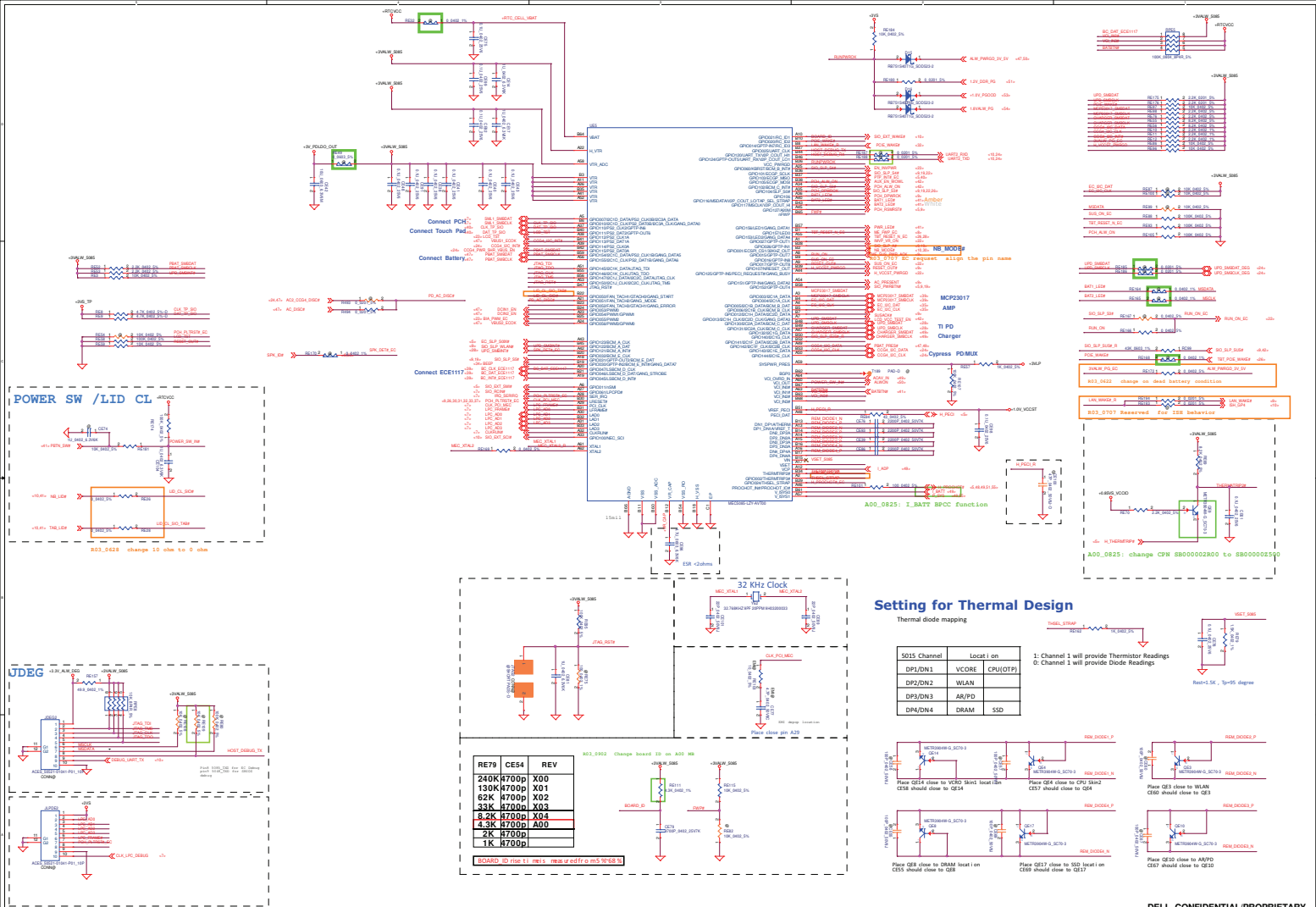
Tom0114:wait CIS symbol
 T#ISOL 158-1160902600
 VDD1=ODR_PWR=3.3V
 VDD2=SD_VDD2=1.8V
 changed footprint & CPN



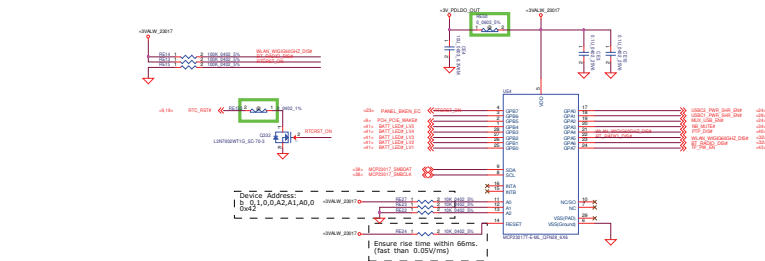
- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closest to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closest to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



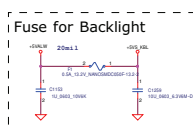
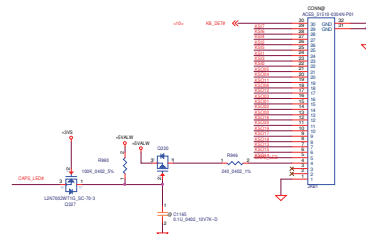
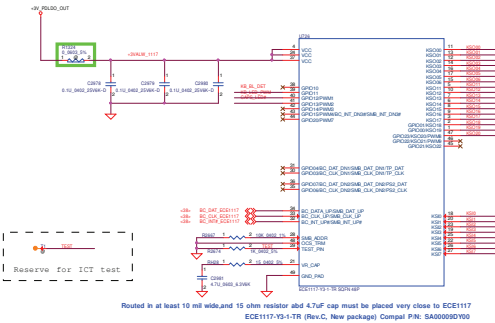
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Date:	Wednesday November 16 2016			Rev 0.1
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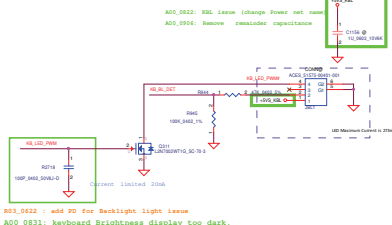
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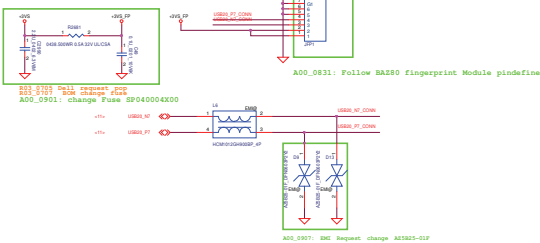
Connector Pin	Keyboard Signal	ECE1117 Pin Name
1	GND	
2	NC	
3	NC	
4	CapLock LED	GPIO3
5	KS010	KS014
6	KS011	KS015
7	KS009	KS013
8	KS014	KS018
9	KS013	KS017
10	KS015	KS019
11	KS016	KS020
12	KS012	KS016
13	KS006	KS008
14	KS002	KS002
15	KS011	KS013
16	KS003	KS003
17	KS008	KS012
18	KS006	KS006
19	KS007	KS013
20	KS004	KS004
21	KS005	KS005
22	KS008	KS008
23	KS013	KS013
24	KS011	KS011
25	KS015	KS015
26	KS012	KS012
27	KS004	KS004
28	KS016	KS016
29	KS017	KS017
30	Omeg_Loop	



Connector for Keyboard Backlight



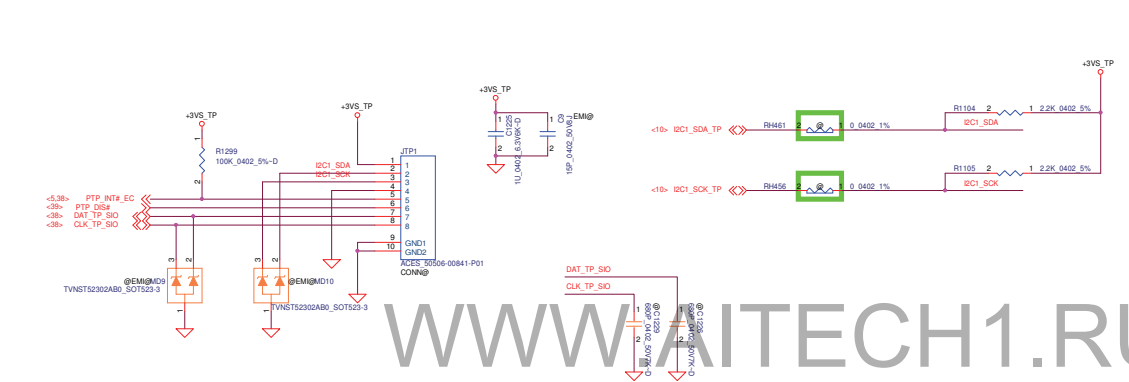
Fingerprint



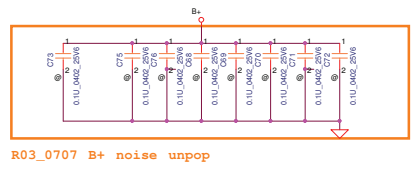
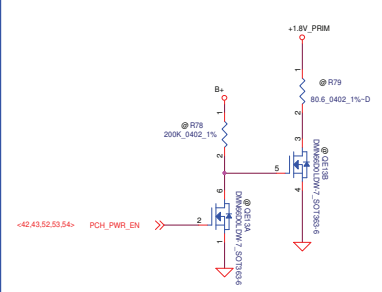
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Secret	Secret	Secret
LA-D781P	LA-D781P	LA-D781P

Touchpad CONN

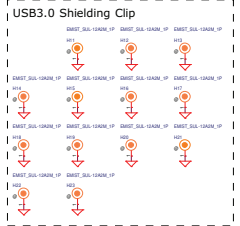
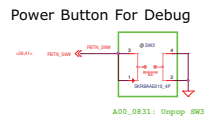
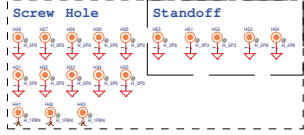


+1.8VA Discharge

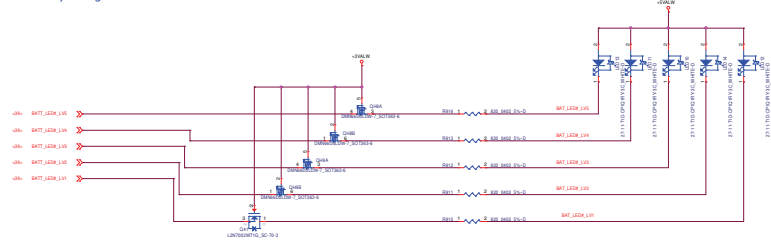


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Title		P36-TP/PWGRD/LID	
Size		Document Number	
LA-D781P		Rev	
Date: Wednesday, November 14, 2018		18mm 40 of 88	

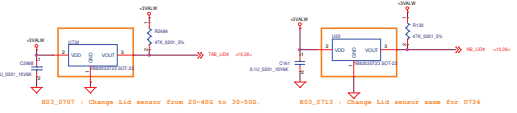


Battery Gauge LED

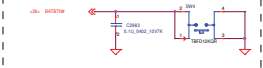


Tablet LID SW

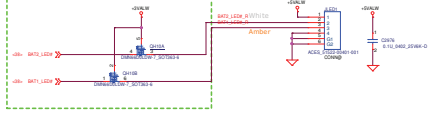
NB LID SW



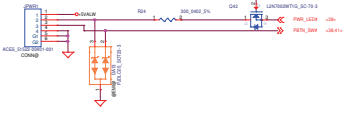
Battery Gauge Button



Connector for Front LED FPC



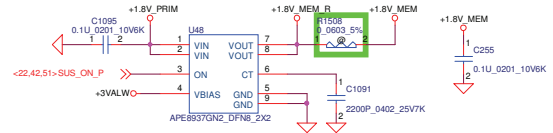
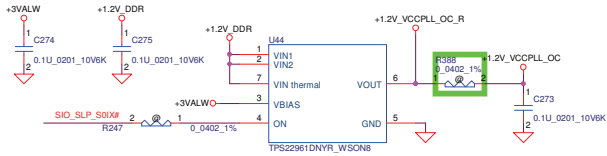
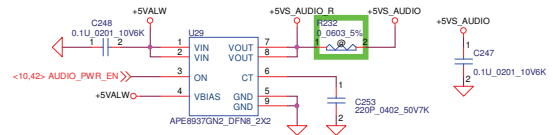
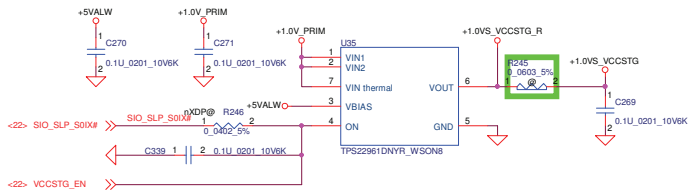
PWR CONN



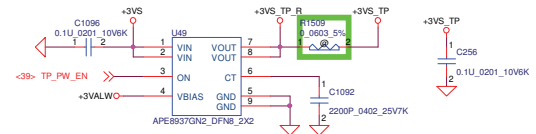
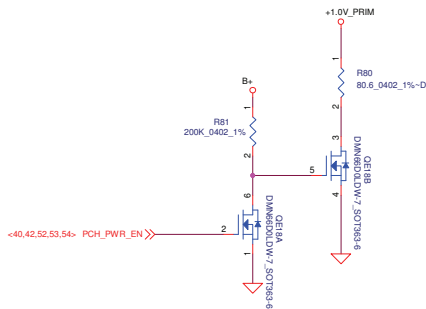
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Secret	Control Secret Data	Control Electronics, Inc.
Secret	Control Secret Data	LA-0781P

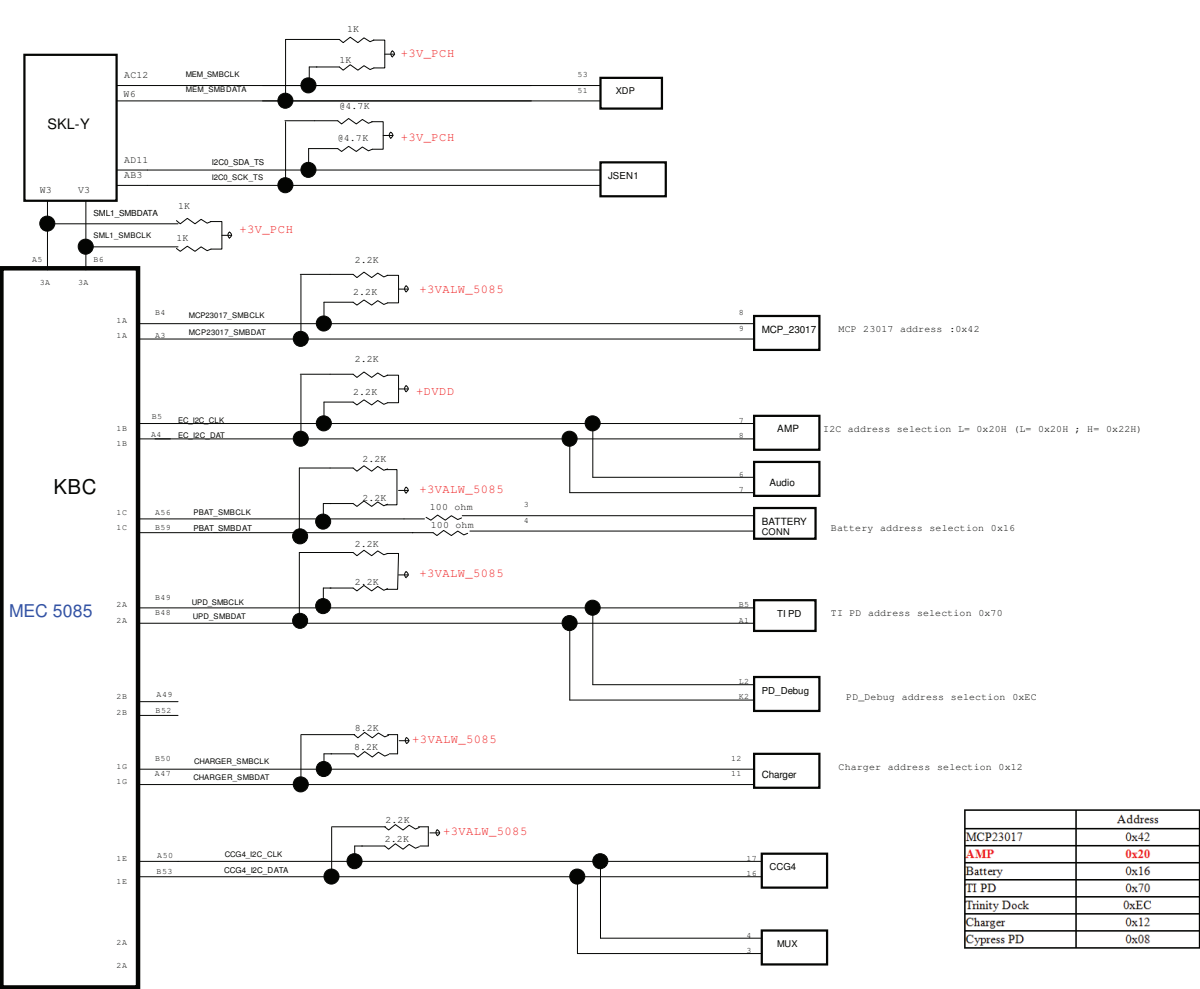
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Size	Unclassified	Number	Rev		0.1
LA-D31P					
Date	Wednesday, November 16, 2016	Sheet	42	of	58



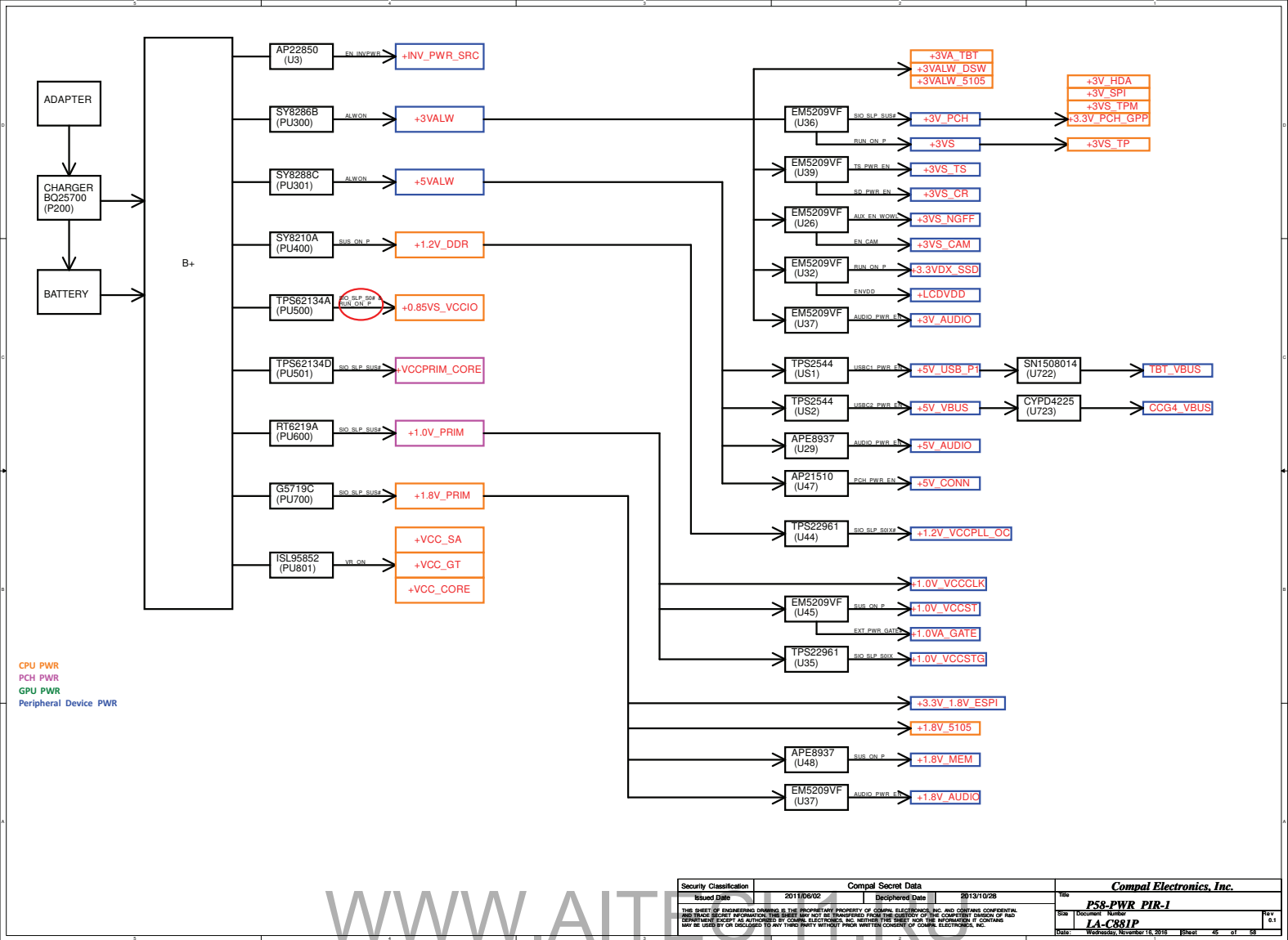
+1.0V_PRIM Discharge

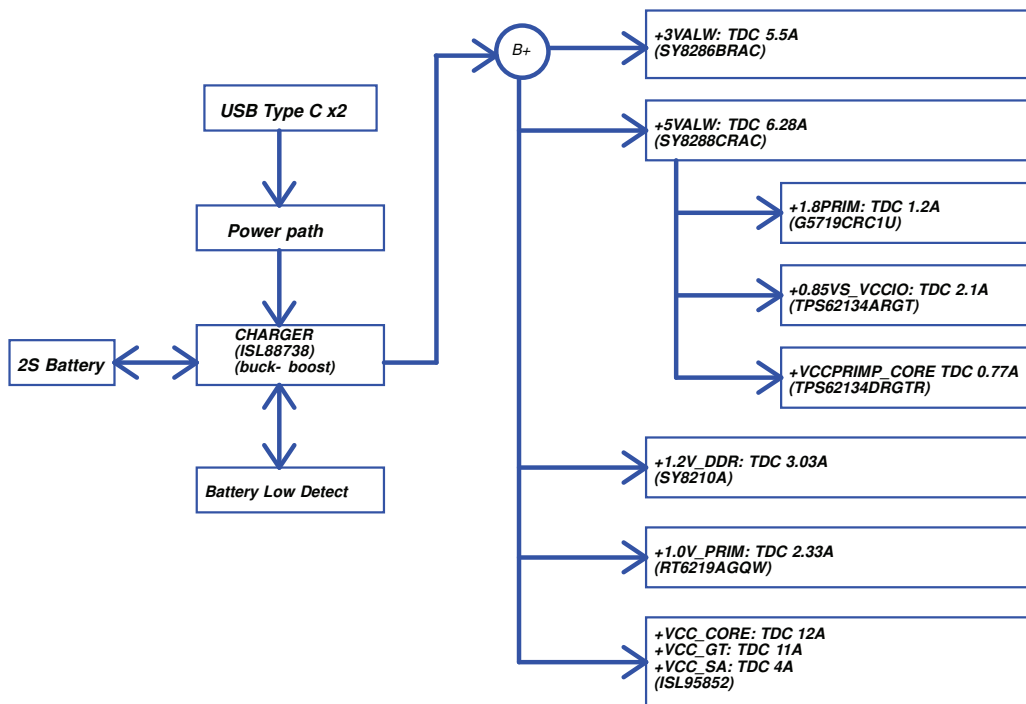


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				LA-D311P	Rev 0.1
				Date:	Wednesday, November 16, 2016
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	Address
MCP23017	0x42
AMP	0x20
Battery	0x16
TI PD	0x70
Trinity Dock	0xEC
Charger	0x12
Cypress PD	0x08

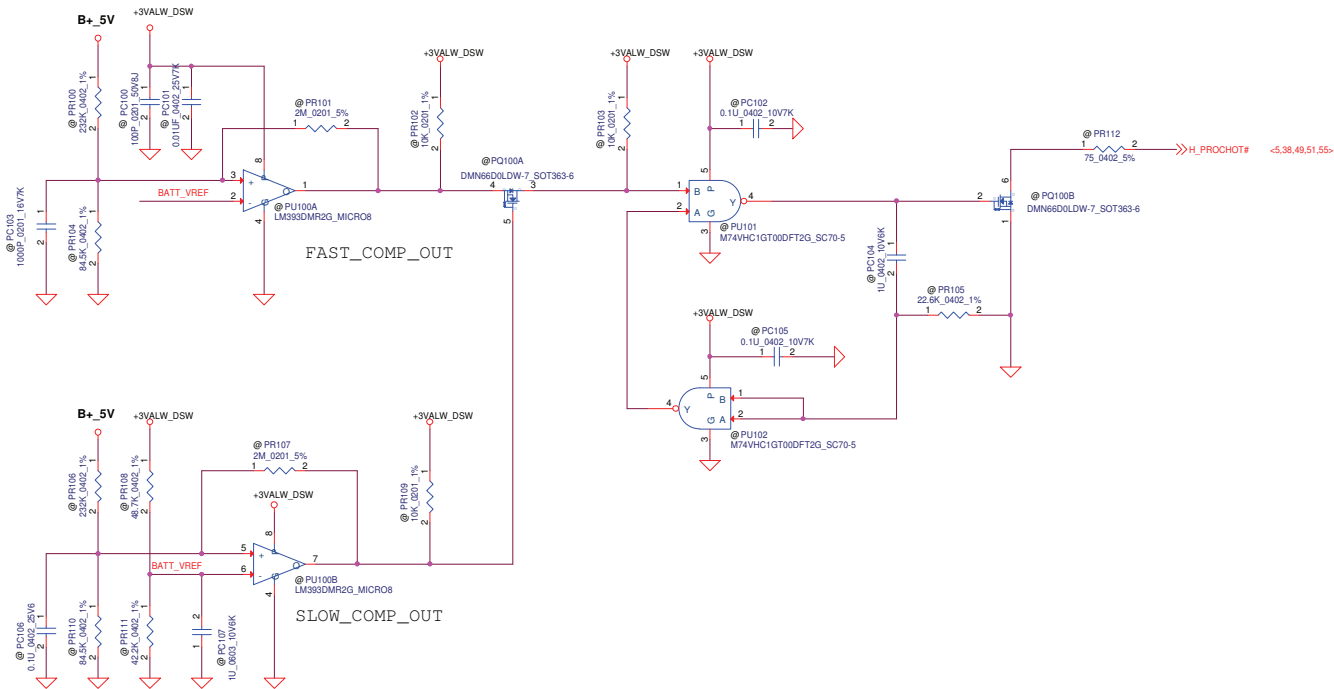




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BATT low voltage detect

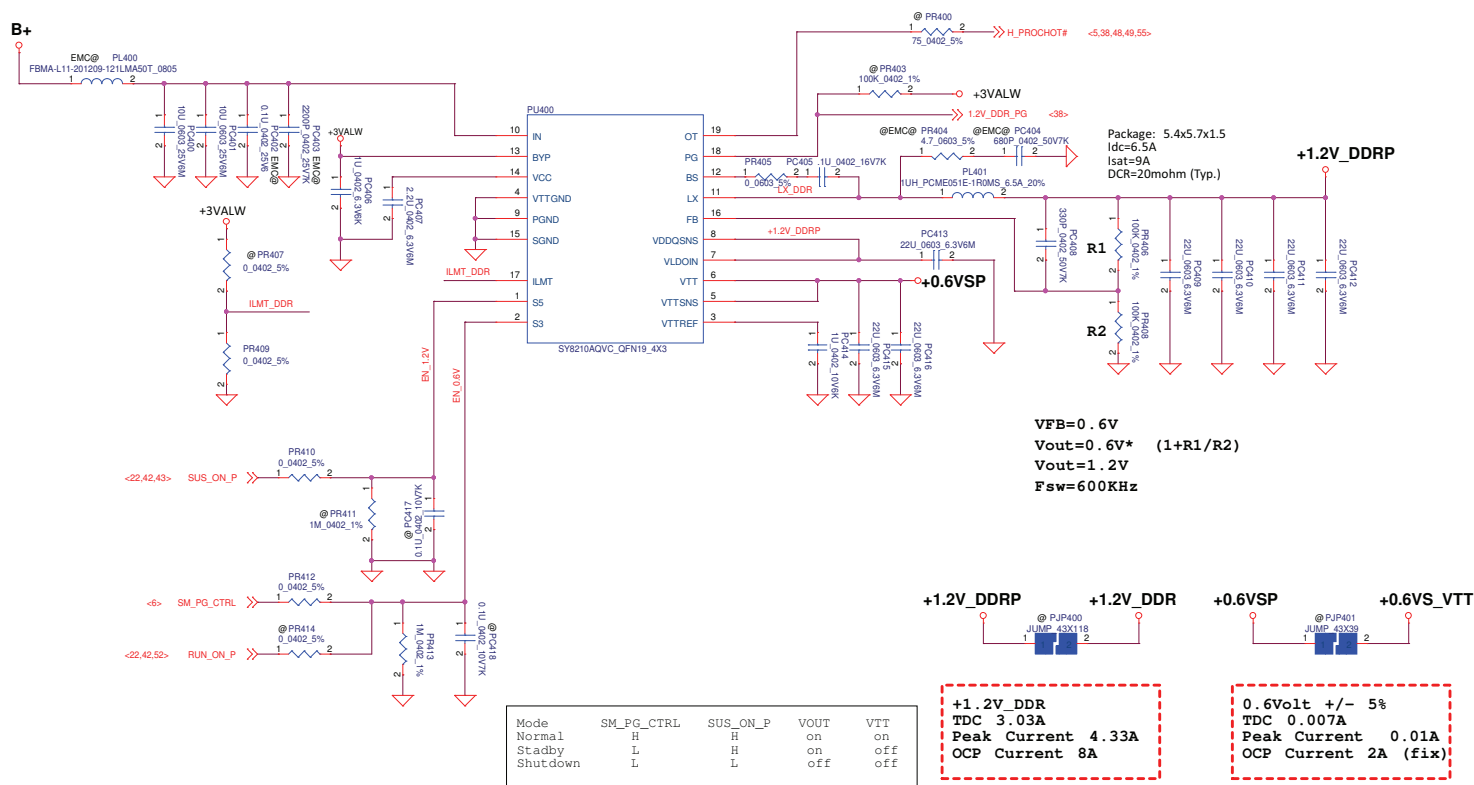


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<p>DATE: 7/28/15 BY: 101501</p>			<p>LA27819</p>	
<p>Sheet 48 of 51</p>			<p>1</p>	

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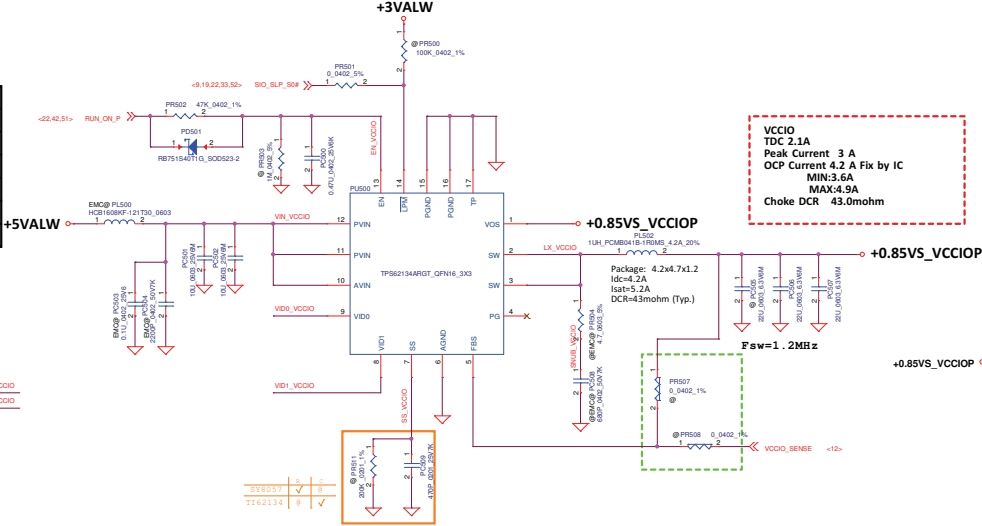
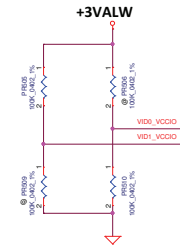


DDR controller(35.3), Support component(35.4)

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				LA-D781P	Rev 0.1
Date: Wednesday, November 16, 2016				Sheet	51 of 56

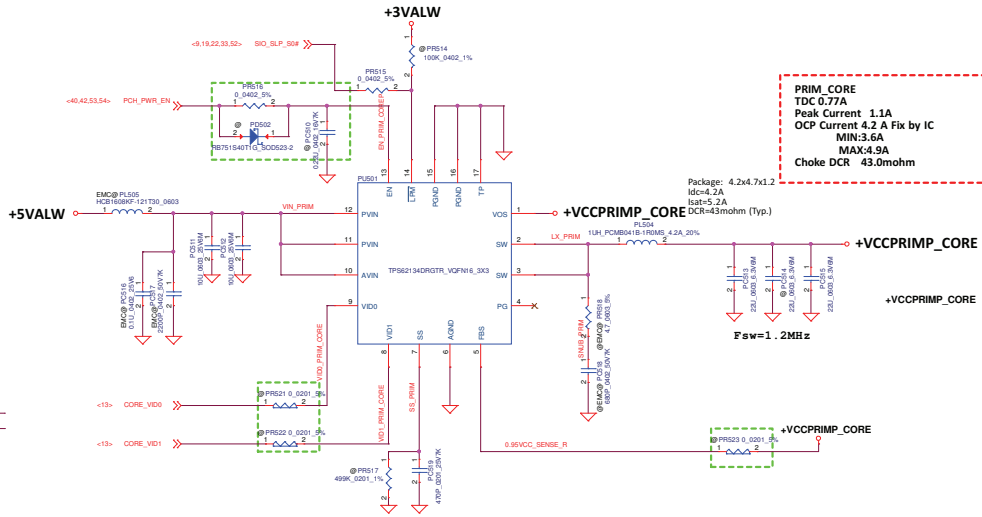
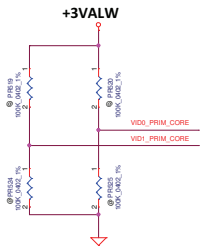
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TPS62134A				
IP	VID1	VID0	Vout(V)	
0	X	X	0.00	
1	0	0	0.850	
1	0	1	0.875	
1	1	0	0.950	
1	1	1	0.975	



VCCIO
TDC 2.1A
Peak Current 3 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 43.0mohm

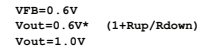
TPS62134D				
IP	VID1	VID0	Vout(V)	
0	X	X	0.700	
1	0	0	0.850	
1	0	1	0.900	
1	1	0	0.950	
1	1	1	1.000	

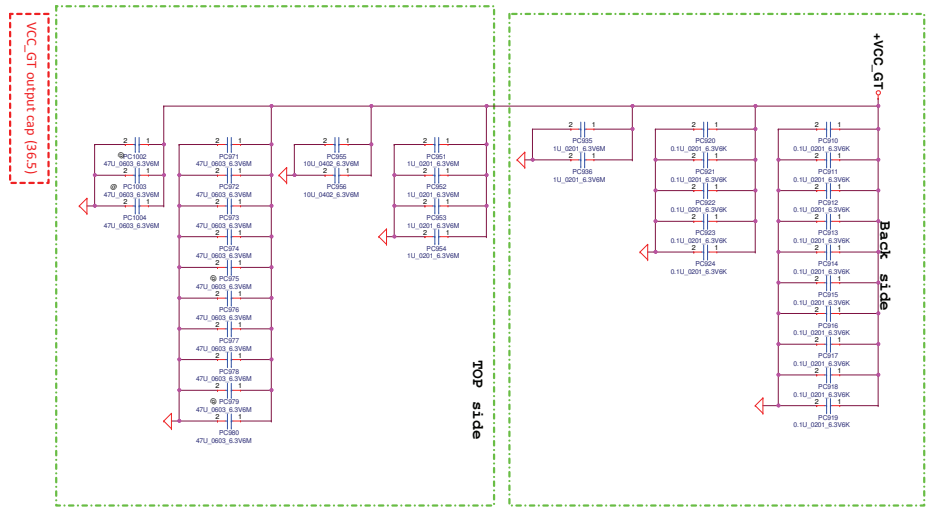
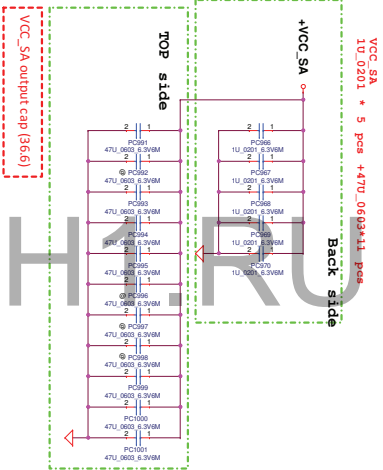
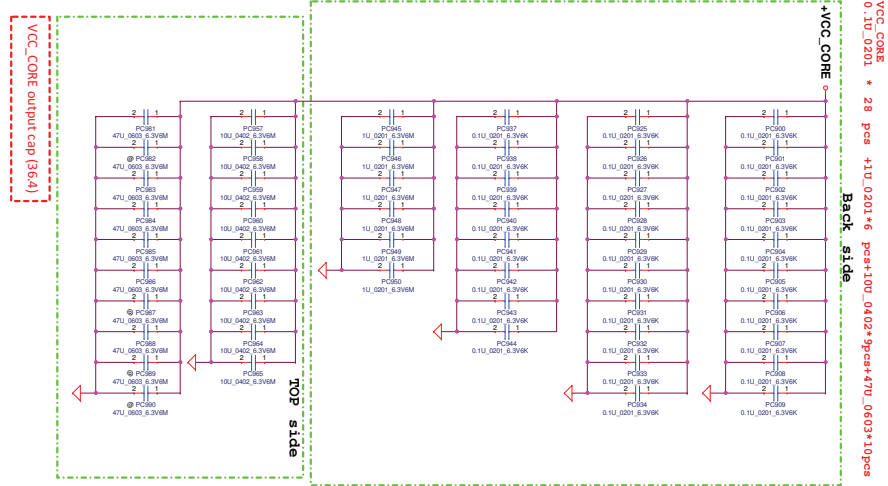


PRIM_CORE
TDC 0.77A
Peak Current 1.1A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 43.0mohm

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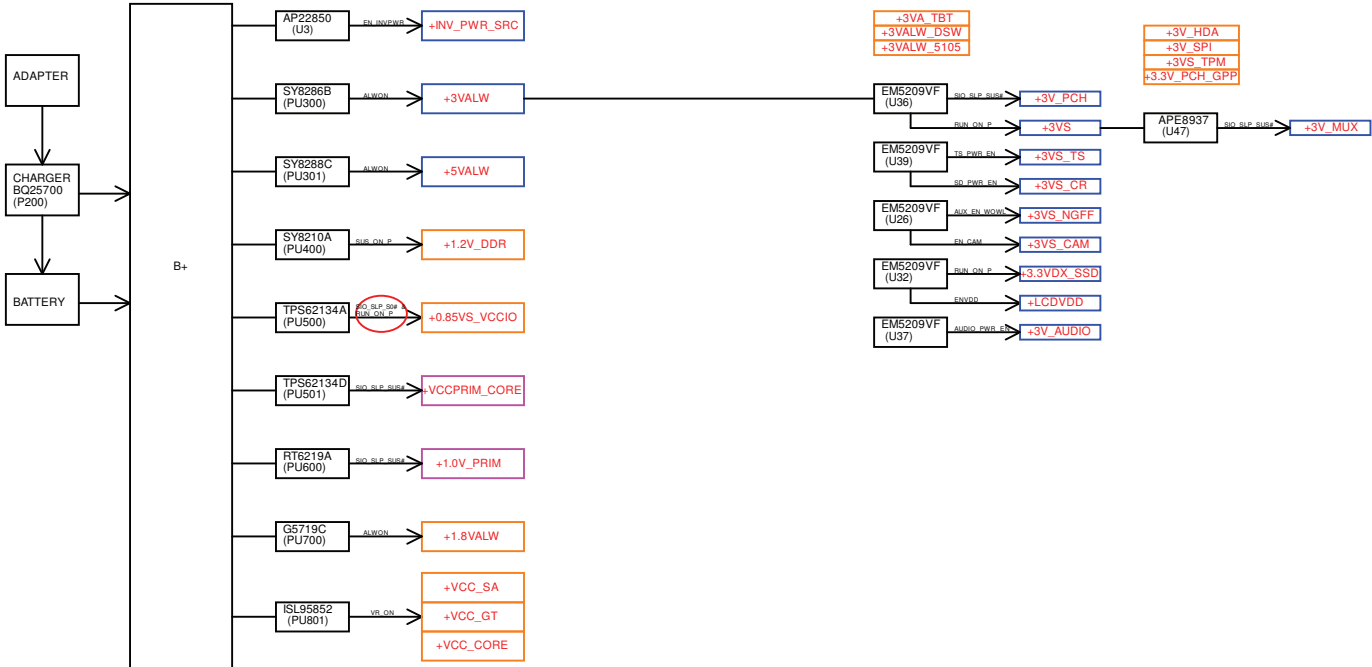
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				Doc Name	REV
				DB-1942P	0.1
				Date	Wednesday, November 18, 2015
				Page	05 of 06





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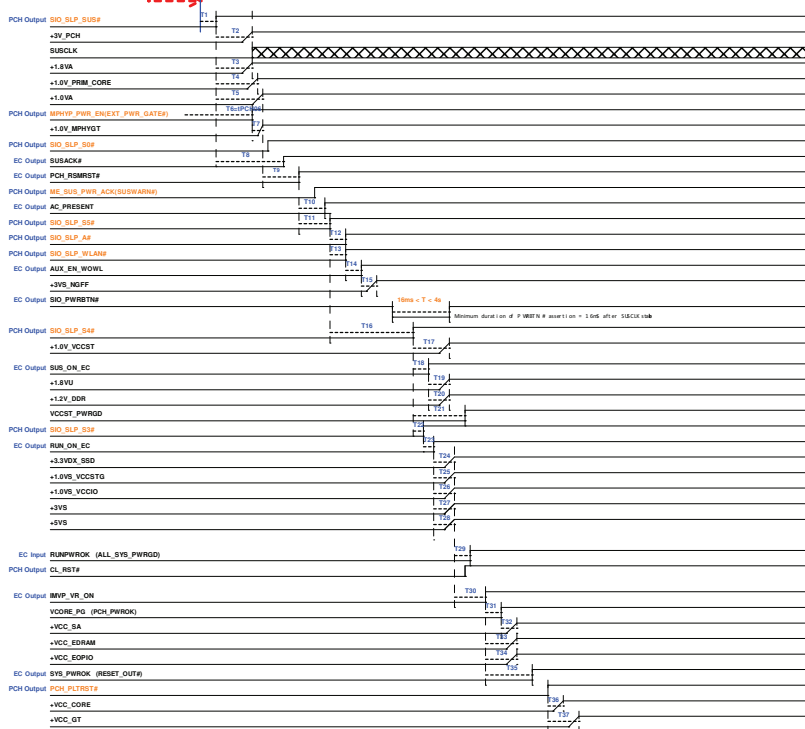
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Rev		Rev	
1-A-17701P		1-A-17701P	
100%		100%	



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			LA-C881P	0.4
			Date	Released: November 18, 2015

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The timing diagram illustrates the sequence of events for the CC04 GPIO. It shows the relationship between several signals: Type-C CCG_VBUS, +3V_POLD0, +3V_POLD0_OUT, CC04 GPIO CCTRL_P1, EC GPIO D0N2_EN, CHD_VIN, B+, ACAV_IN, ALWON, +3VALWP, and +3VALWP. Key timing parameters are indicated: T_{pd} (propagation delay), T_{d} (delay), T_{H} (high pulse width), T_{L} (low pulse width), and $T_{\text{H}} + T_{\text{L}} + 4\mu\text{s}$ (total pulse width). The diagram shows the signals transitioning between high and low states, with the EC GPIO D0N2_EN signal being the primary control signal.



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+VOC_CORE
VGATE

SYS_PWROK
PCH_PLTRST#

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